International
IOR Rectifier

Data Sheet No. PD-6.018D

IR2121

CURRENT LIMITING LOW SIDE DRIVER

Features

- Gate drive supply range from 12 to 18V
- Undervoltage lockout
- Current detection and limiting loop to limit driven power transistor current
- Error lead indicates fault conditions and programs shutdown time
- Output in phase with input

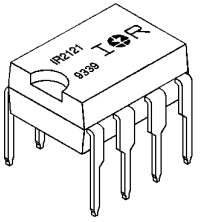
Product Summary

V_{OFFSET}	5V max.
I_O+/-	1A / 2A
V_{OUT}	12 - 18V
V_{CSth}	230 mV
$t_{on/off}$ (typ.)	150 & 150 ns

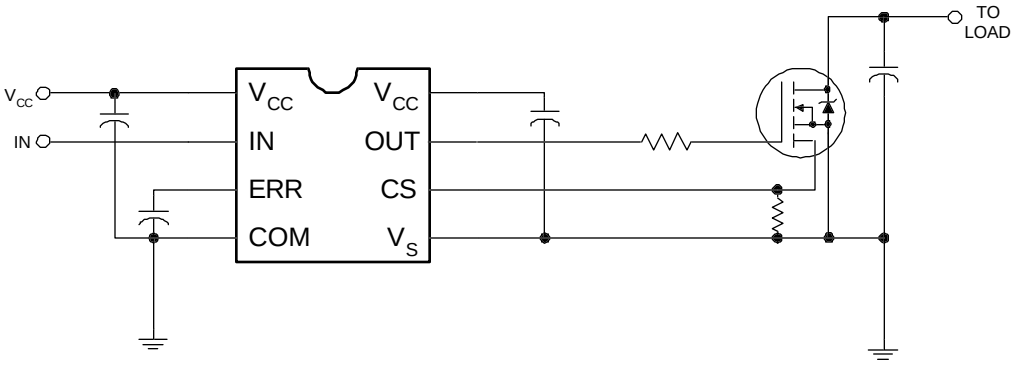
Description

The IR2121 is a high speed power MOSFET and IGBT driver with over-current limiting protection circuitry. Latch immune CMOS technology enables ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output driver features a high pulse current buffer stage designed for minimum cross-conduction. The protection circuitry detects over-current in the driven power transistor and limits the gate drive voltage. Cycle-by-cycle shutdown is programmed by an external capacitor which directly controls the time interval between detection of the over-current limiting condition and latched shutdown. The output can be used to drive an N-channel power MOSFET or IGBT in the low side configuration.

Package



Typical Connection



Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	-0.3	25	V
V_S	Gate Drive Return Voltage	V_{CC} - 25	V_{CC} + 0.3	
V_O	Output Voltage	V_S - 0.3	V_{CC} + 0.3	
V_{IN}	Logic Input Voltage	-0.3	V_{CC} + 0.3	
V_{ERR}	Error Signal Voltage	-0.3	V_{CC} + 0.3	
V_{CS}	Current Sense Voltage	V_S - 0.3	V_{CC} + 0.3	
P_D	Package Power Dissipation @ $T_A \leq +25°C$	—	1.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	—	125	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

Parameter		Value		
Symbol	Definition	Min.	Max.	Units
V_{CC}	Fixed Supply Voltage	V_S + 10	V_S + 20	V
V_S	Gate Drive Return Voltage	-5	5	
V_O	Output Voltage	V_S	V_{CC}	
V_{IN}	Logic Input Voltage	0	V_{CC}	
V_{ERR}	Error Signal Voltage	0	V_{CC}	
V_{CS}	Current Sense Signal Voltage	V_S	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V, C_L = 3300 pF and T_A = 25°C unless otherwise specified. The dynamic electrical characteristics are defined in Figures 2 through 5.

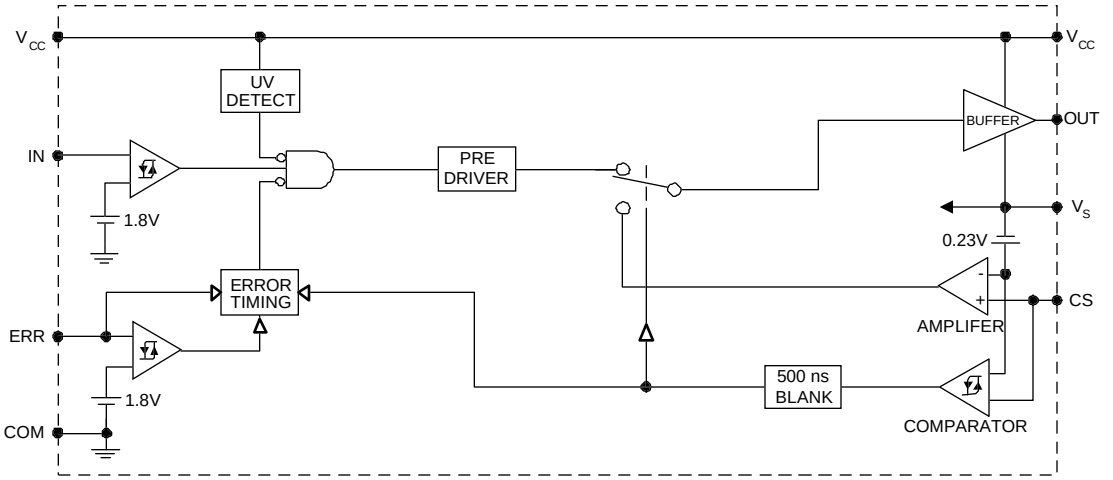
Symbol	Parameter Definition	Figure	Value Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-On Propagation Delay	7	—	150	200	ns	
t_{off}	Turn-Off Propagation Delay	8	—	150	190		
t_{sd}	ERR Shutdown Propagation Delay	9	—	1.7	2.2	µs	
t_r	Turn-On Rise Time	10	—	43	60	ns	
t_f	Turn-Off Fall Time	11	—	26	35		
t_{cs}	CS Shutdown Propagation Delay	12	—	0.7	1.2	µs	
t_{err}	CS to ERR Pull-Up Propagation Delay	13	—	9.0	12		C_{ERR} = 270 pF

Static Electrical Characteristics

V_{BIAS} (V_{CC}) = 15V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to V_S .

Symbol	Parameter Definition	Figure	Value Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	14	2.2	—	—	V	V_{CC} = 12V to 18V
V_{IL}	Logic "0" Input Voltage	15	—	—	0.8		V_{CC} = 12V to 18V
V_{CSTH+}	CS Input Positive Going Threshold	16	150	230	320	mV	V_{CC} = 12V to 18V
V_{CSTH-}	CS Input Negative Going Threshold	17	130	200	260		V_{CC} = 12V to 18V
V_{OH}	High Level Output Voltage, V_{BIAS} - V_O	18	—	—	100		I_O = 0A
V_{OL}	Low Level Output Voltage, V_O	19	—	—	100		I_O = 0A
I_{QCC}	Quiescent V_{CC} Supply Current	20	—	1.1	2.2	mA	V_{IN} = V_{CS} = 0V or 5V
I_{IN+}	Logic "1" Input Bias Current	21	—	4.5	10	µA	V_{IN} = 5V
I_{IN-}	Logic "0" Input Bias Current	22	—	—	1.0		V_{IN} = 0V
I_{CS+}	"High" CS Bias Current	23	—	4.5	10		V_{CS} = 3V or 5V
I_{CS-}	"Low" CS Bias Current	24	—	—	1.0		V_{CS} = 0V
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	25	8.3	8.9	9.6	V	
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	26	7.3	8.0	8.7		
I_{ERR}	ERR Timing Charge Current	27	65	100	130	µA	V_{IN} = 5V, V_{CS} = 3V ERR < V_{ERR+}
I_{ERR+}	ERR Pull-Up Current	28	8.0	15	—	mA	V_{IN} = 5V, V_{CS} = 3V ERR > V_{ERR+}
I_{ERR-}	ERR Pull-Down Current	29	16	30	—		V_{IN} = 0V
I_{O+}	Output High Short Circuit Pulsed Current	30	1.0	1.6	—	A	V_O = 0V, V_{IN} = 5V PW ≤ 10 µs
I_{O-}	Output Low Short Circuit Pulsed Current	31	2.0	3.3	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

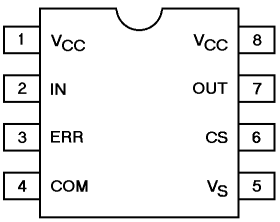
Functional Block Diagram



Lead Definitions

Lead Symbol	Description
V_{CC}	Logic and gate drive supply
IN	Logic input for gate driver output (OUT), in phase with OUT
ERR	Serves multiple functions; status reporting, linear mode timing and cycle by cycle logic shutdown
COM	Logic ground
OUT	Gate drive output
V_S	Gate drive supply return
CS	Current sense input to current sense comparator

Lead Assignments

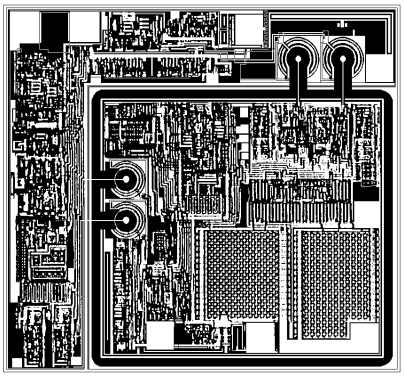


8 Lead DIP

IR2121

Part Number

Device Information

Process & Design Rule			HVDCMOS 4.0 µm
Transistor Count			410
Die Size			104 X 111 X 26 (mil)
Die Outline			
Thickness of Gate Oxide			800Å
Connections		Material	Poly Silicon
	First Layer	Width	4 µm
		Spacing	6 µm
		Thickness	5000Å
		Material	Al - Si (Si: 1.0% ±0.1%)
	Second Layer	Width	6 µm
		Spacing	9 µm
		Thickness	20,000Å
Contact Hole Dimension			8 µm X 8 µm
Insulation Layer		Material	PSG (SiO_2)
		Thickness	1.5 µm
Passivation (1)		Material	PSG (SiO_2)
		Thickness	1.5 µm
Passivation (2)		Material	Proprietary*
		Thickness	Proprietary*
Method of Saw			Full Cut
Method of Die Bond			Ablebond 84 - 1
Wire Bond		Method	Thermo Sonic
		Material	Au (1.0 mil / 1.3 mil)
Leadframe		Material	Cu
		Die Area	Ag
		Lead Plating	Pb : Sn (37 : 63)
Package		Types	8 Lead PDIP
		Materials	EME6300 / MP150 / MP190

Remarks: * Patent Pending

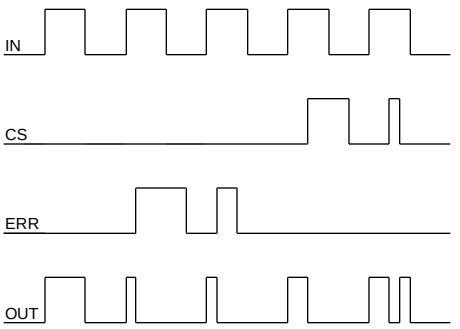


Figure 1. Input/Output Timing Diagram

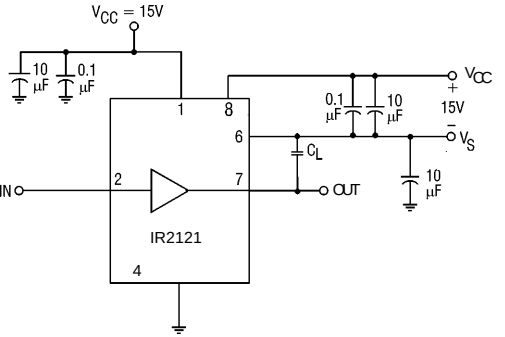


Figure 2. Switching Time Test Circuit

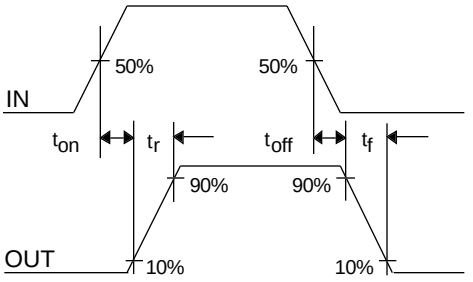


Figure 3. Switching Time Waveform Definitions

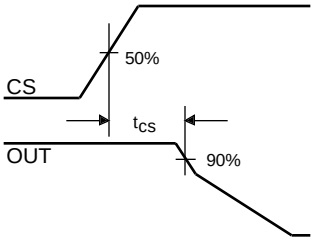


Figure 4. ERR Shutdown Waveform Definitions

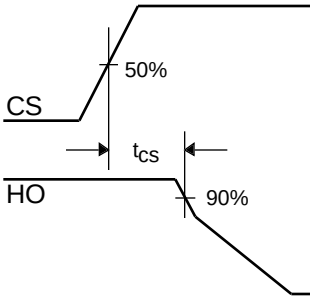


Figure 5. CS Shutdown Waveform Definitions

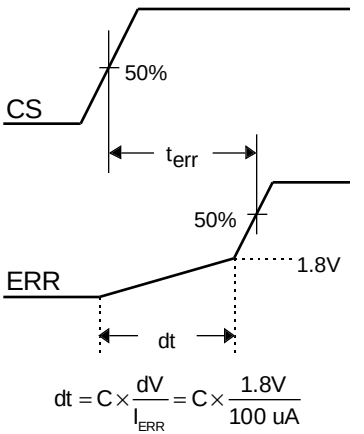


Figure 6. CS to ERR Waveform Definitions

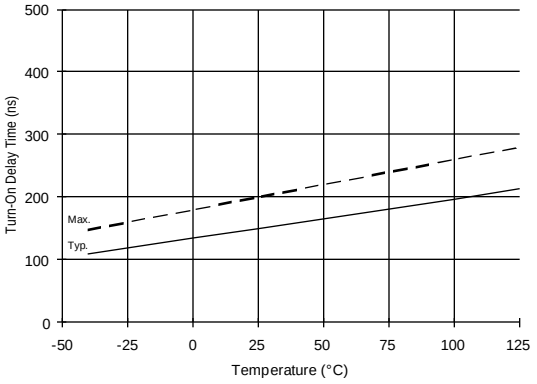


Figure 7A. Turn-On Time vs. Temperature

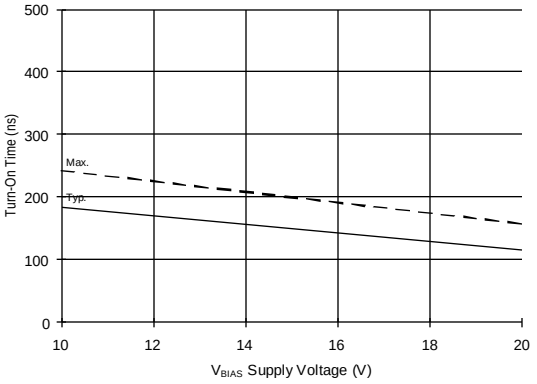


Figure 7B. Turn-On Time vs. Voltage

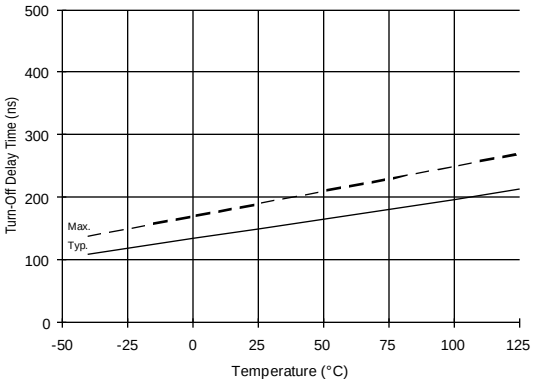


Figure 8A. Turn-Off Time vs. Temperature

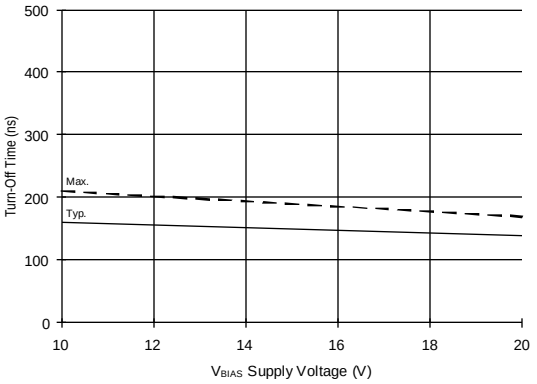


Figure 8B. Turn-Off Time vs. Voltage

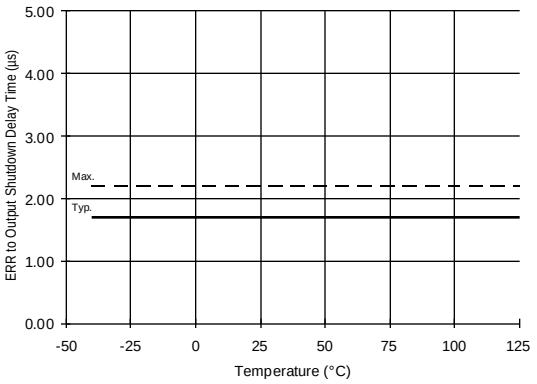


Figure 9A. ERR to Output Shutdown vs. Temperature

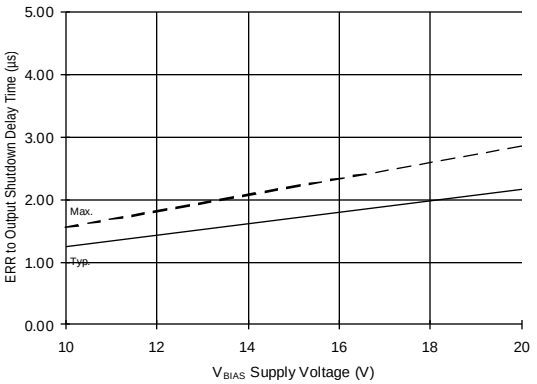


Figure 9B. ERR to Output Shutdown vs. Voltage

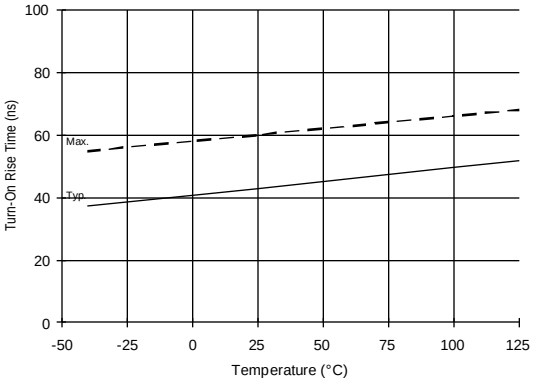


Figure 10A. Turn-On Rise Time vs. Temperature

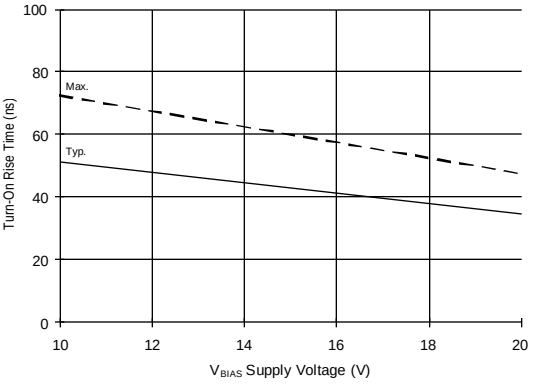


Figure 10B. Turn-On Rise Time vs. Voltage

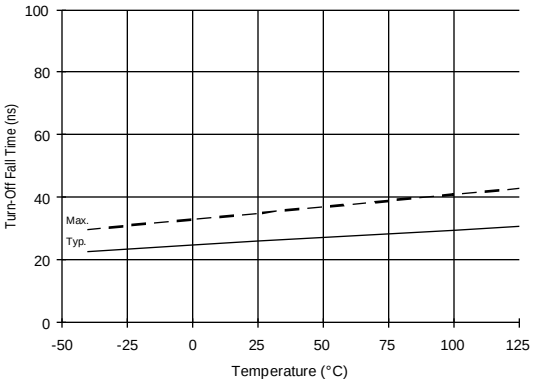


Figure 11A. Turn-Off Fall Time vs. Temperature

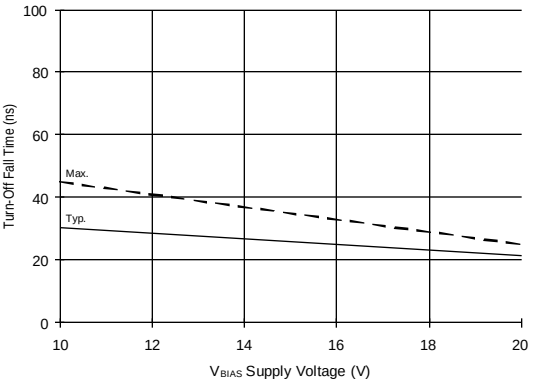


Figure 11B. Turn-Off Fall Time vs. Voltage

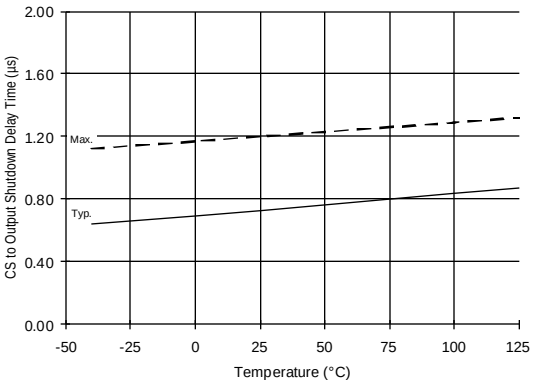


Figure 12A. CS to Output Shutdown vs. Temperature

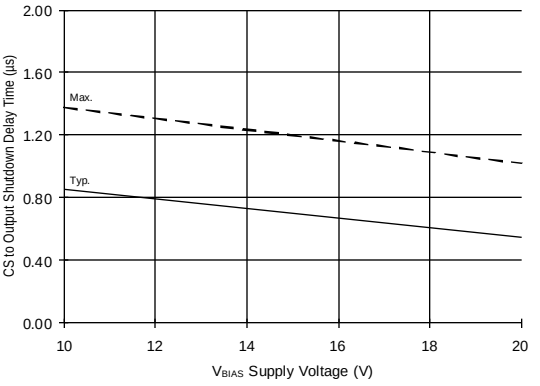


Figure 12B. CS to Output Shutdown vs. Voltage

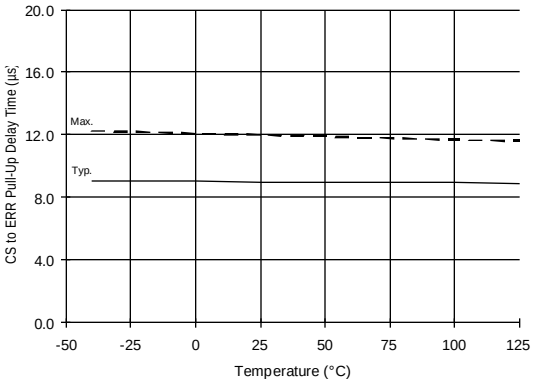


Figure 13A. CS to ERR Pull-Up vs. Temperature

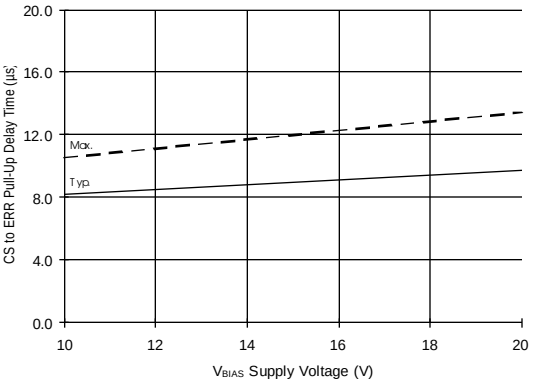


Figure 13B. CS to ERR Pull-Up vs. Voltage

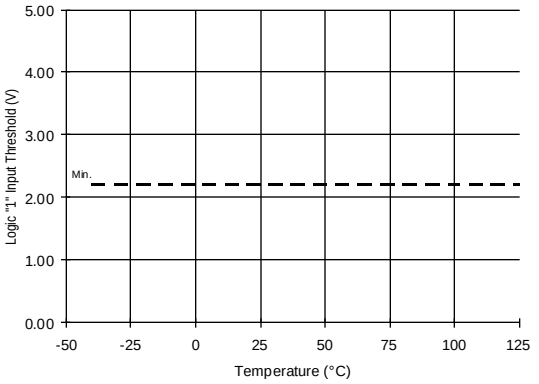


Figure 14A. Logic "1" Input Threshold vs. Temperature

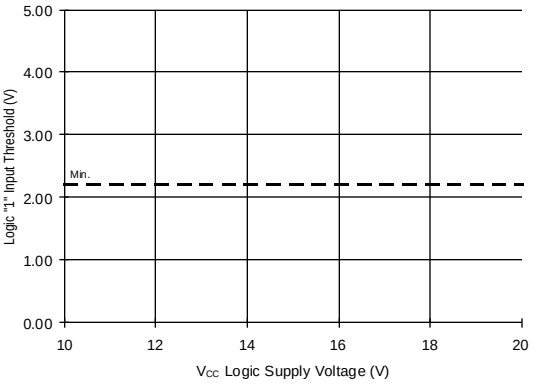


Figure 14B. Logic "1" Input Threshold vs. Voltage

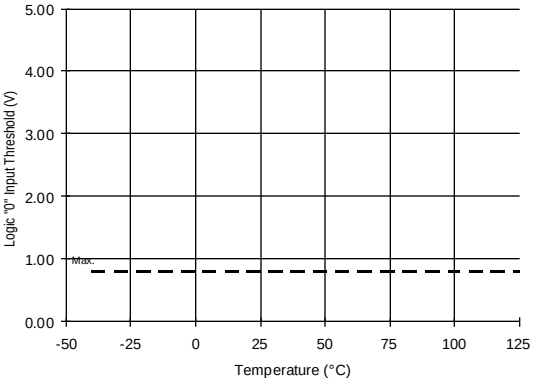


Figure 15A. Logic "0" Input Threshold vs. Temperature

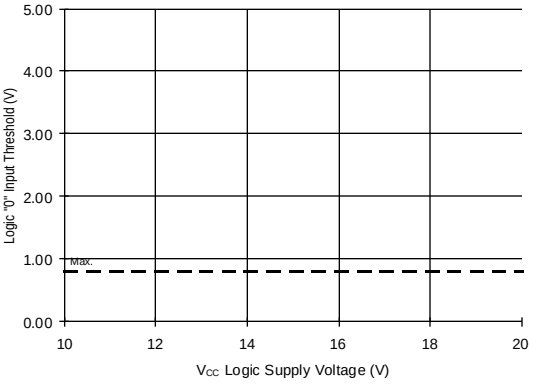


Figure 15B. Logic "0" Input Threshold vs. Voltage

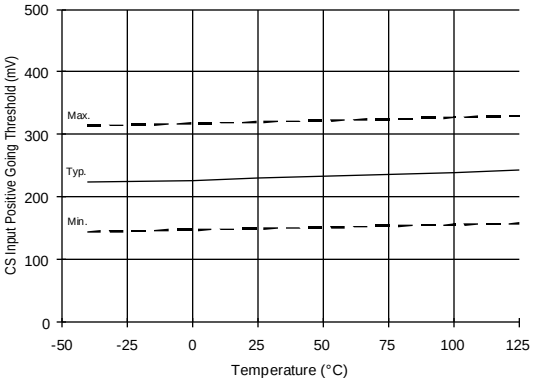


Figure 16A. CS Input Threshold (+) vs. Temperature

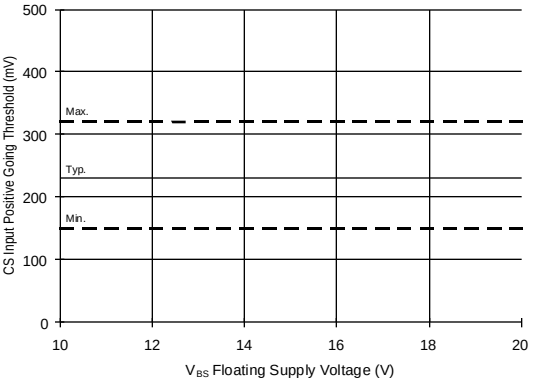


Figure 16B. CS Input Threshold (+) vs. Voltage

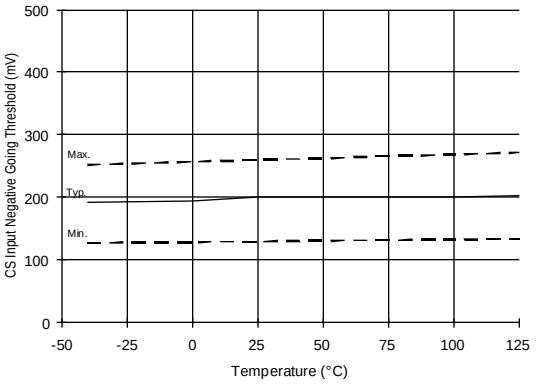


Figure 17A. CS Input Threshold (-) vs. Temperature

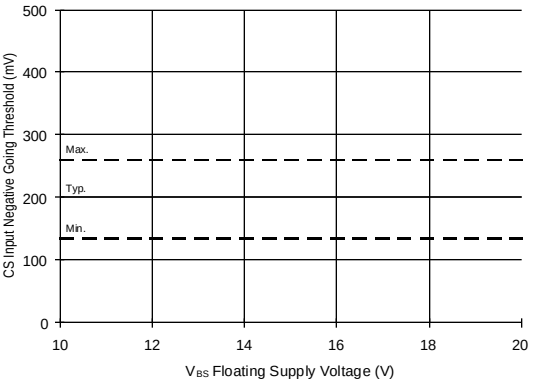


Figure 17B. CS Input Threshold (-) vs. Voltage

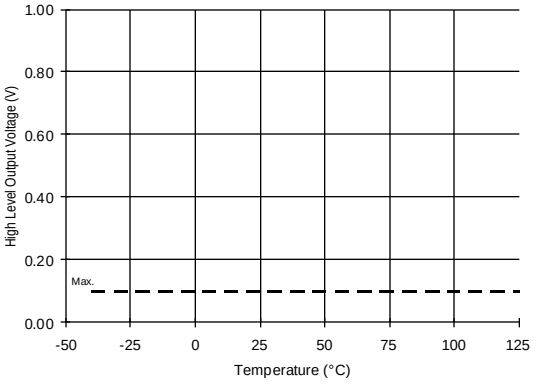


Figure 18A. High Level Output vs. Temperature

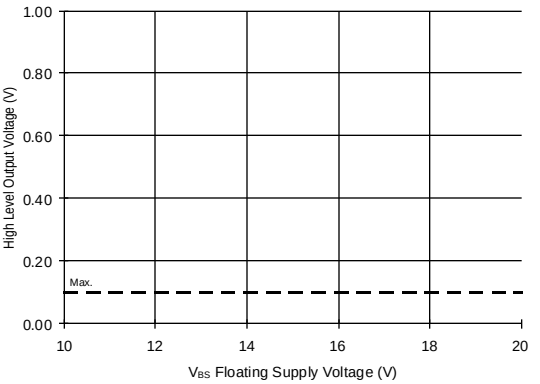


Figure 18B. High Level Output vs. Voltage

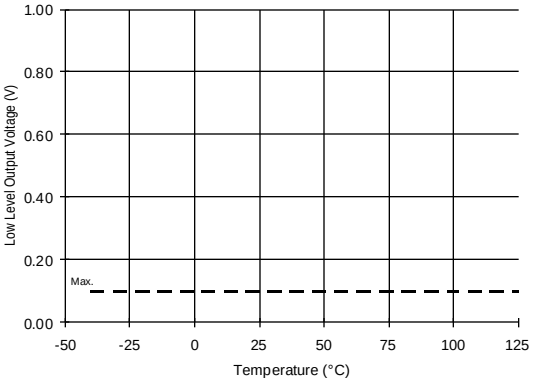


Figure 19A. Low Level Output vs. Temperature

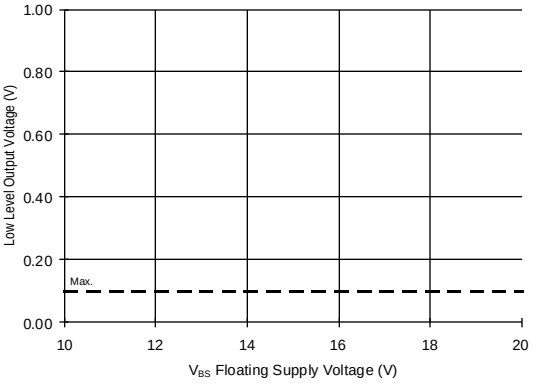


Figure 19B. Low Level Output vs. Voltage

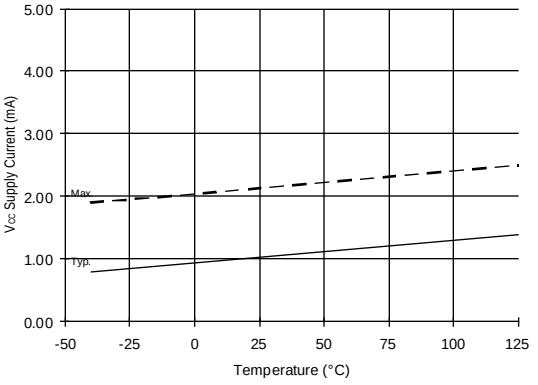


Figure 20A. V_{CC} Supply Current vs. Temperature

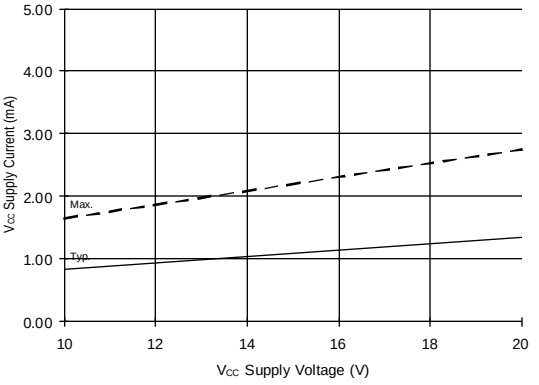


Figure 20B. V_{CC} Supply Current vs. Voltage

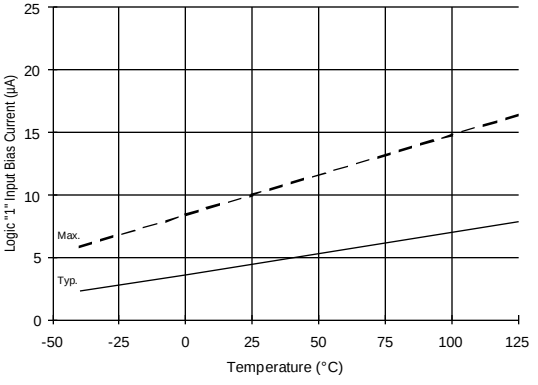


Figure 21A. Logic "1" Input Current vs. Temperature

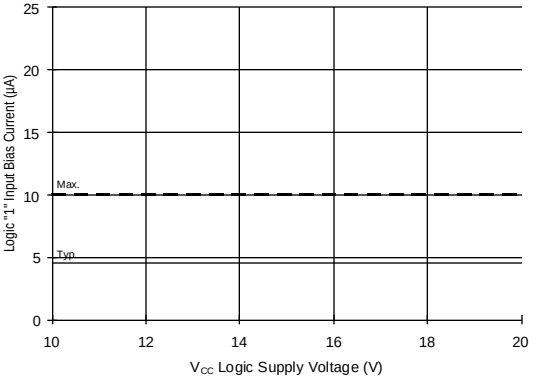


Figure 21B. Logic "1" Input Current vs. Voltage

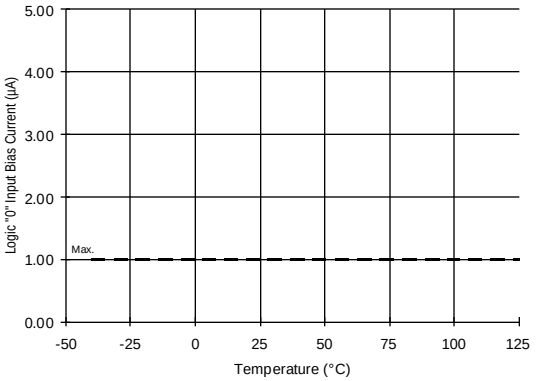


Figure 22A. Logic "0" Input Current vs. Temperature

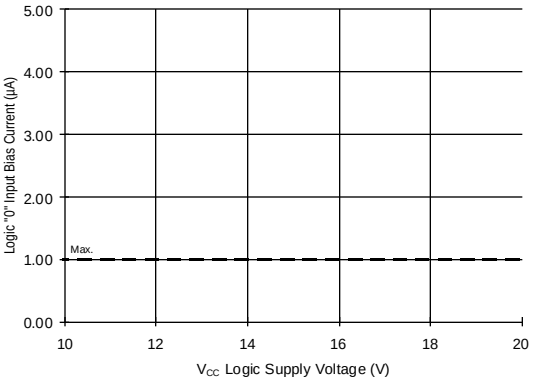


Figure 22B. Logic "0" Input Current vs. Voltage

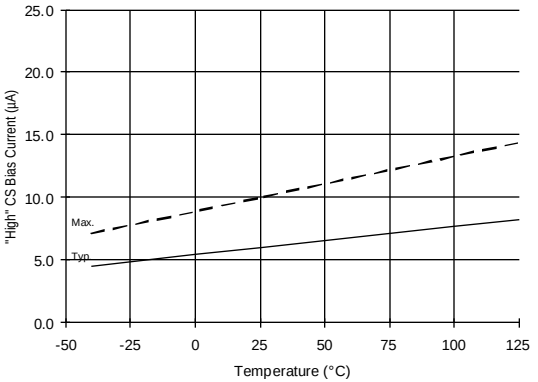


Figure 23A. "High" CS Bias Current vs. Temperature

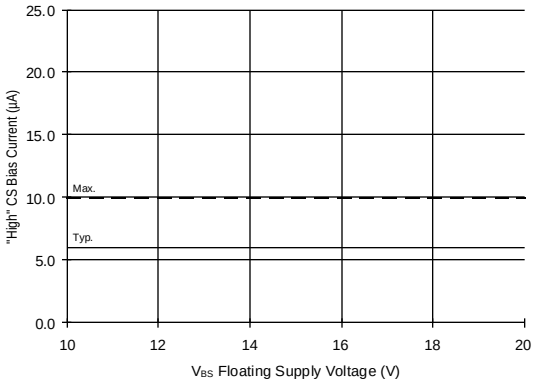


Figure 23B. "High" CS Bias Current vs. Voltage

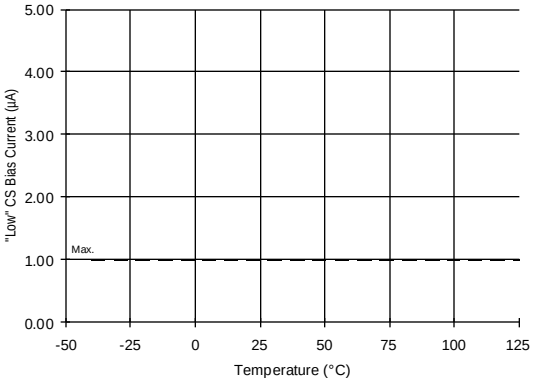


Figure 24A. "Low" CS Bias Current vs. Temperature

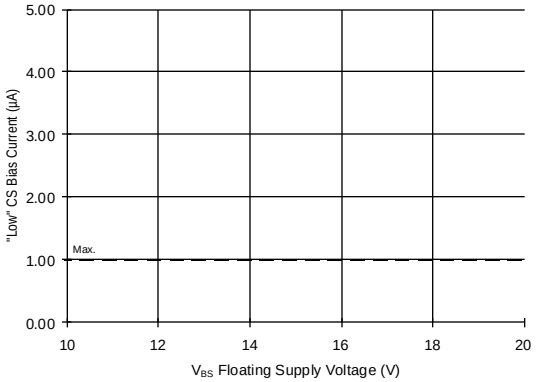


Figure 24B. "Low" CS Bias Current vs. Voltage

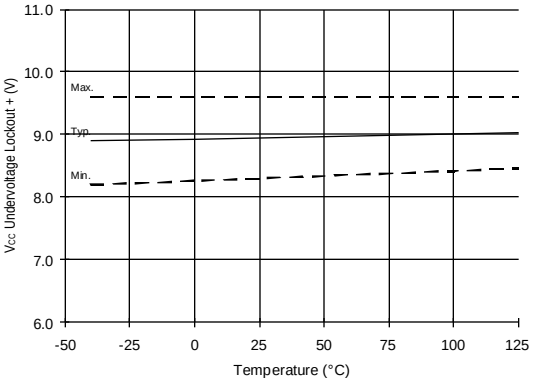


Figure 25. V_{CC} Undervoltage (+) vs. Temperature

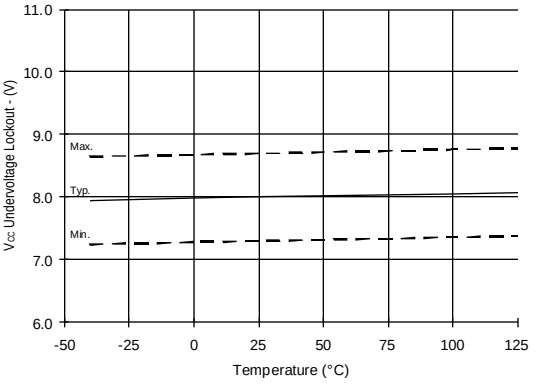


Figure 26. V_{CC} Undervoltage (-) vs. Temperature

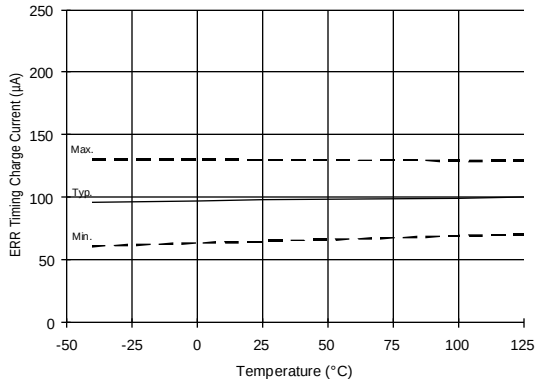


Figure 27A. ERR Timing Charge Current vs. Temperature

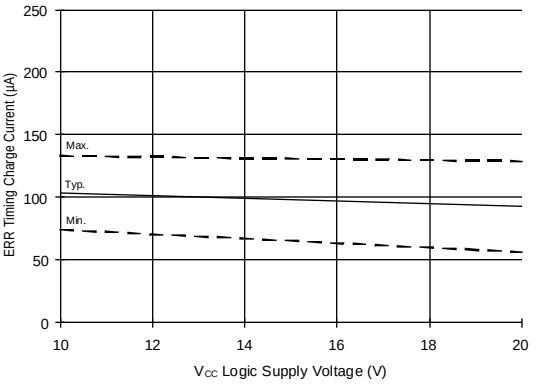


Figure 27B. ERR Timing Charge Current vs. Voltage

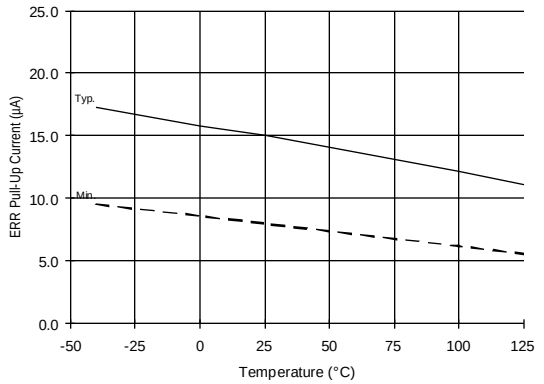


Figure 28A. ERR Pull-Up Current vs. Temperature

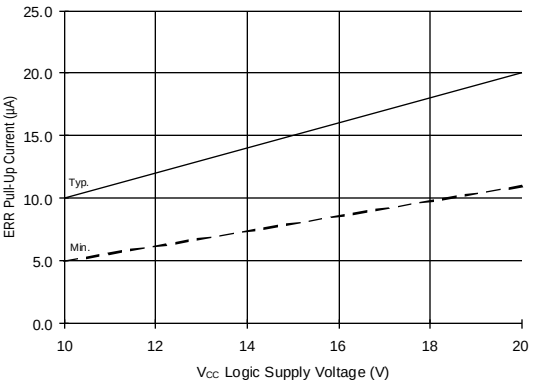


Figure 28B. ERR Pull-Up Current vs. Voltage

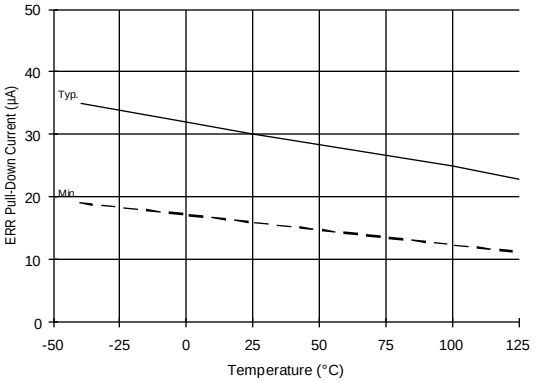


Figure 29A. ERR Pull-Down Current vs.Temperature

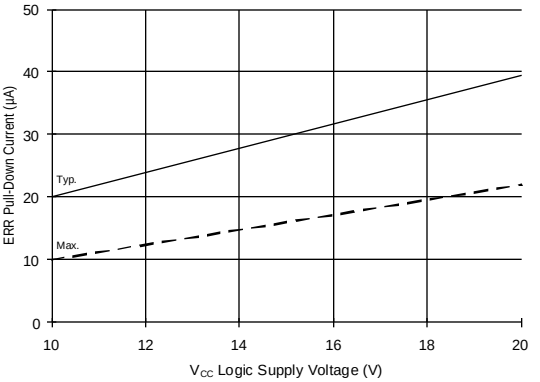


Figure 29B. ERR Pull-Down Current vs. Voltage

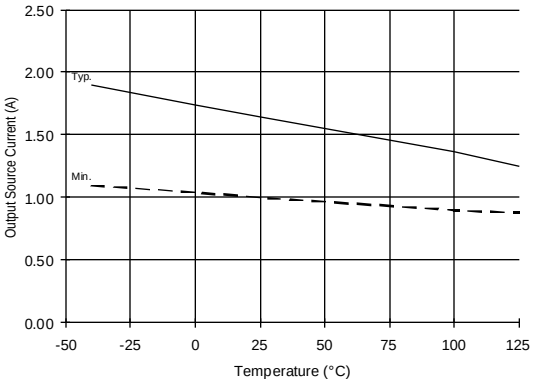


Figure 30A. Output Source Current vs.Temperature

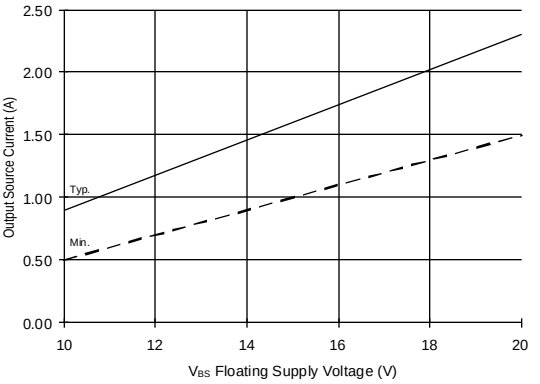


Figure 30B. Output Source Current vs. Voltage

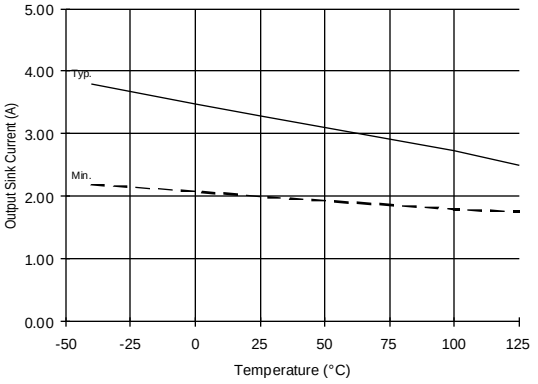


Figure 31A. Output Sink Current vs.Temperature

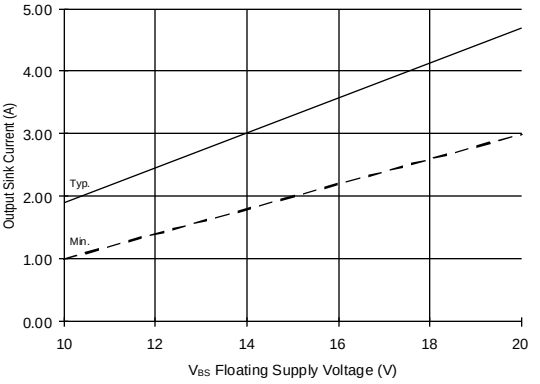


Figure 31B. Output Sink Current vs. Voltage

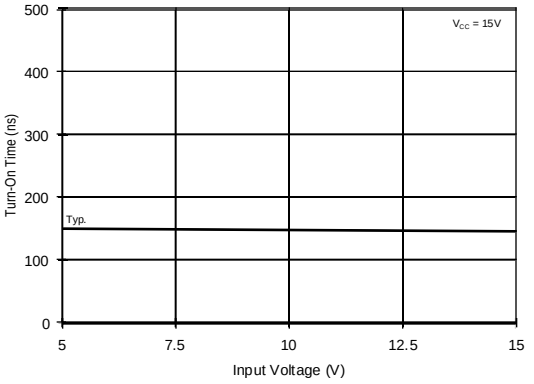


Figure 32A. Turn-On Time vs. Input Temperature

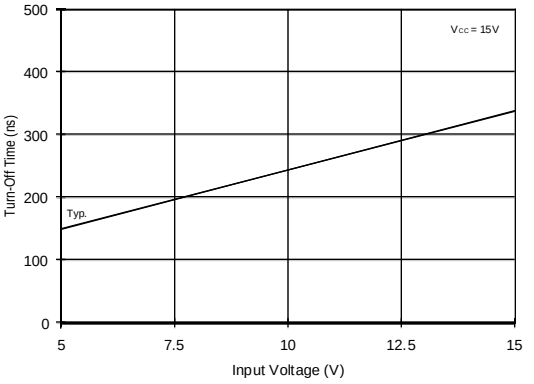


Figure 32B. Turn-Off Time vs. Input Voltage

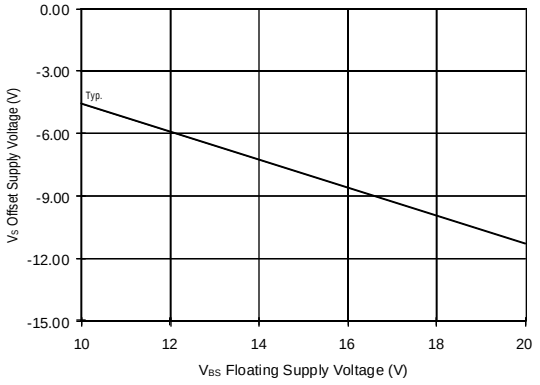


Figure 33. Maximum V_S Negative Offset vs. Supply Voltage