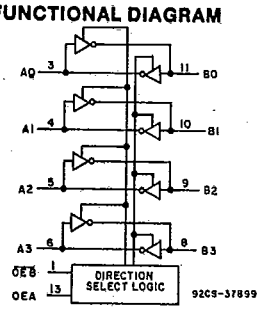
T-52-31-00

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

File Number **1488**

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



CD54/74HC242, HCT242

Quad-Bus Transceiver with 3-State Outputs

Type Features:

- *Typical propagation delay (A←→B) of 7 ns @ V_{CC} = 5 V C_L = 15 pF, T_A = 25° C*
- *3-state outputs*
- *Buffered inputs*

The RCA-CD54/74HC242, 243 and CD54/74HCT242, 243 silicon-gate CMOS 3-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads.

The CD54/74HC242 and CD54/74HCT242 are inverting buffers; the CD54/74HC243 and CD54/74HCT243 are non-inverting buffers.

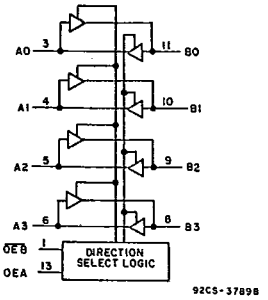
The states of the output enables ($\overline{OEB}$, OEA) determine both the direction of flow (A to B, B to A), and the 3-state mode.

The CD54HC242, 243 and CD54HCT242, 243 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC242, 243 and CD74HCT242, 243 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

FUNCTIONAL DIAGRAM



CD54/74HC243, HCT243

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

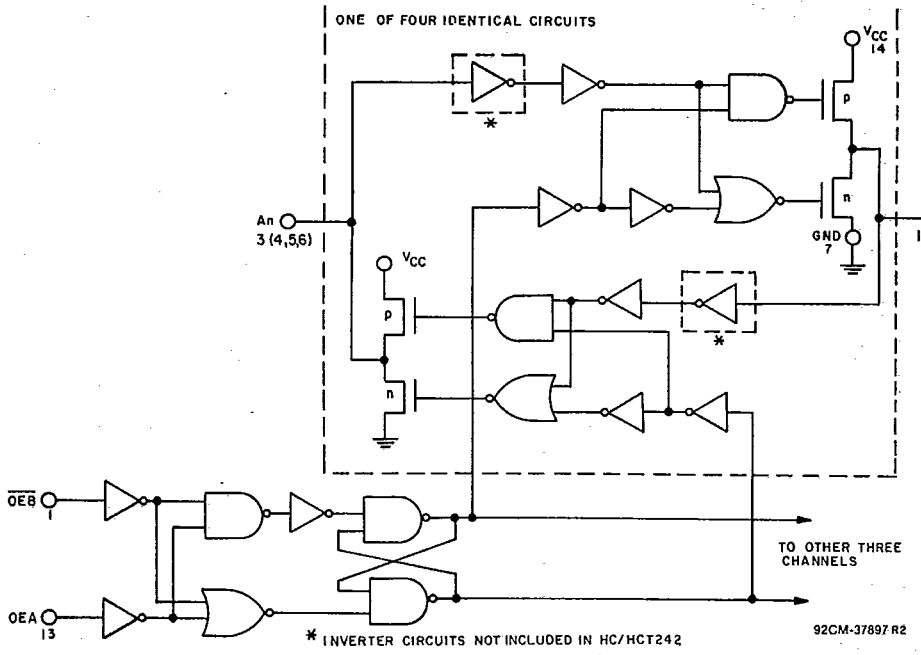


Fig. 1 - Logic diagram for the CD54/74HC/HCT242, 243.

TRUTH TABLE

CONTROL INPUTS		HC, HCT242 Series		HC, HCT243 Series	
		DATA PORT STATUS		DATA PORT STATUS	
$\overline{OEB}$	OEA	A_n	B_n	A_n	B_n
H	H	$\overline{O}$	I	O	I
L	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	L	I	$\overline{O}$	I	O

H = High
L = Low
I = Input

O = Output (Same Level as Input)
$\overline{O}$ = Output (Inversion of Input Level)
Z = High Impedance

To prevent excess currents in the High Z modes all I/O terminals should be terminated with 10 kΩ to 1 MΩ resistors.

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) ..... ±35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±70 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC242/243/CD54HC242/243										CD74HCT242/243/CD54HCT242/243									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State Leakage Current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5.0	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5.0	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
An, Bn	1.1
OEA, $\overline{OEB}$	0.6

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

T-52-31

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L pF	Typical				UNITS
			HC242	HCT242	HC243	HCT243	
Propagation Delay Data to Output	t_{PHL} t_{PLH}	15	7	8	7	9	ns
Enable to High Z	t_{PHZ}, t_{PLZ}	15	12	14	12	14	ns
Enable from High-Z	t_{PZH}, t_{PZL}	15	12	14	12	14	ns
Power Dissipation Capacitance*	C_{PD}	—	85	90	80	91	pF

*C_{PD} is used to determine the dynamic power consumption, per channel.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
Data to Outputs	t_{PHL}	4.5	—	18	—	20	—	23	—	25	—	27	—	30	ns
HC/HCT242		6	—	15	—	—	—	20	—	—	—	23	—	—	
Propagation Delay	t_{PLH}	2	—	90	—	—	—	115	—	—	—	135	—	—	
Data to Outputs	t_{PHL}	4.5	—	18	—	22	—	23	—	28	—	27	—	33	ns
for HC/HCT243		6	—	15	—	—	—	20	—	—	—	23	—	—	
Output High-Z:	t_{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	
to High Level;	t_{PZL}	4.5	—	30	—	34	—	38	—	43	—	45	—	51	ns
to Low Level		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output High Level;	t_{PHZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
Output Low Level to High-Z	t_{PLZ}	4.5	—	30	—	35	—	38	—	44	—	45	—	53	ns
		6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

CD54/74HC242, CD54/74HCT242
CD54/74HC243, CD54/74HCT243

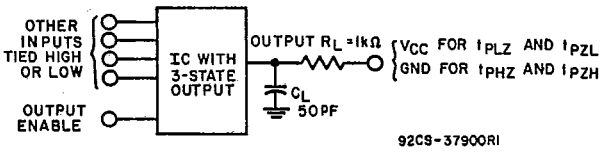
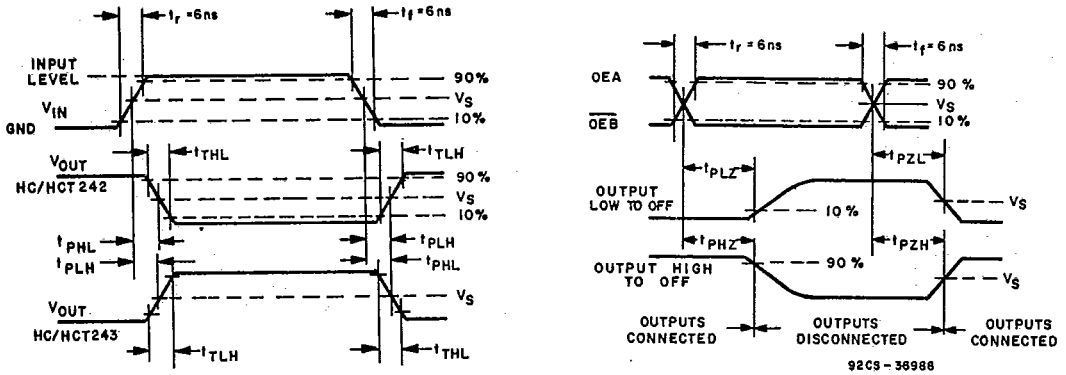
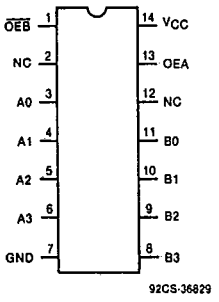


Fig. 2 - Three-state propagation delay test circuit.



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

Fig. 3 - Transition times and propagation delay times.



TERMINAL ASSIGNMENT

ORDERING INFORMATION

RCA CMOS device packages are identified by letters indicated in the following chart. When ordering a CMOS device, it is important that the appropriate suffix letter be affixed to the type number of the device.

Package	Suffix Letter
Dual-In-Line Plastic	E
Dual-In-Line Frit-Seal Ceramic	F
Dual-In-Line Surface Mount Plastic	M
Chip	H

The CD54HC/HCT series is supplied in dual-in-line frit-seal ceramic packages (F suffix). The CD74HC/HCT series is supplied in dual-in-line plastic packages (E suffix) and in dual-in-line surface mount plastic packages (M suffix). Both series are supplied in chip form (H suffix).

For example, a CD54HC242 will be identified as the CD54HC242F. The CD74HC242 will be identified as the CD74HC242E.