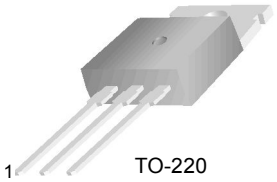
FAIRCHILD SEMICONDUCTOR®

October 2008

TIP120/TIP121/TIP122

NPN Epitaxial Darlington Transistor

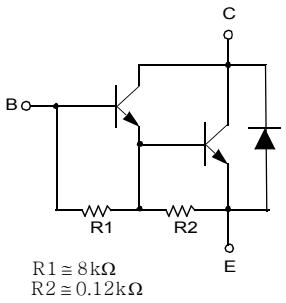
- Medium Power Linear Switching Applications
- Complementary to TIP125/126/127



TO-220

1.Base 2.Collector 3.Emitter

Equivalent Circuit



$R1 \cong 8k\Omega$
$R2 \cong 0.12k\Omega$

Absolute Maximum Ratings* T_a = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{CBO}	Collector-Base Voltage : TIP120 : TIP121 : TIP122	60 80 100	V V V
V_{CEO}	Collector-Emitter Voltage : TIP120 : TIP121 : TIP122	60 80 100	V V V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current (DC)	5	A
I_{CP}	Collector Current (Pulse)	8	A
I_B	Base Current (DC)	120	mA
P_C	Collector Dissipation (T_a=25°C)	2	W
	Collector Dissipation (T_C=25°C)	65	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 65 ~ 150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

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Electrical Characteristics* T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage : TIP120 : TIP121 : TIP122	 I_C = 100mA, I_B = 0	 60 80 100			 V V V
I_{CEO}	Collector Cut-off Current : TIP120 : TIP121 : TIP122	 V_{CE} = 30V, I_B = 0 V_{CE} = 40V, I_B = 0 V_{CE} = 50V, I_B = 0			 0.5 0.5 0.5	 mA mA mA
I_{CBO}	Collector Cut-off Current : TIP120 : TIP121 : TIP122	 V_{CB} = 60V, I_E = 0 V_{CB} = 80V, I_E = 0 V_{CB} = 100V, I_E = 0			 0.2 0.2 0.2	 mA mA mA
I_{EBO}	Emitter Cut-off Current	V_{BE} = 5V, I_C = 0			2	mA
h_{FE}	* DC Current Gain	V_{CE} = 3V,I_C = 0.5A V_{CE} = 3V, I_C = 3A	1000 1000			
V_{CE}(sat)	* Collector-Emitter Saturation Voltage	I_C = 3A, I_B = 12mA I_C = 5A, I_B = 20mA			2.0 4.0	V V
V_{BE}(on)	* Base-Emitter On Voltage	V_{CE} = 3V, I_C = 3A			2.5	V
C_{ob}	Output Capacitance	V_{CB} = 10V, I_E = 0, f = 0.1MHz			200	pF

* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

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Typical characteristics

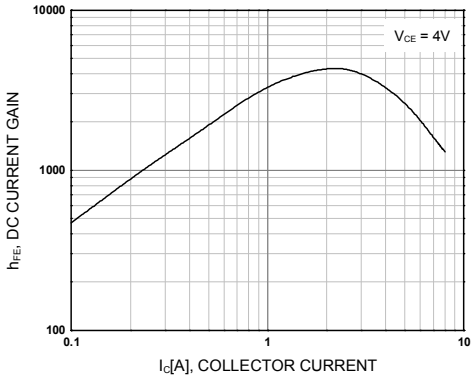

Figure 1. DC current Gain

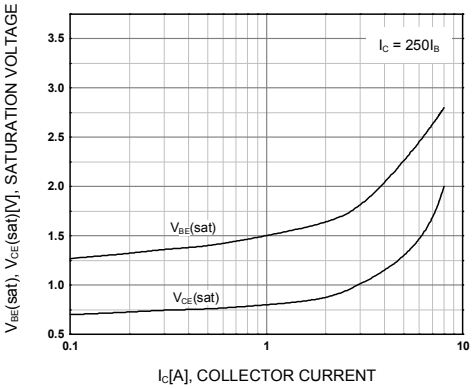

Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

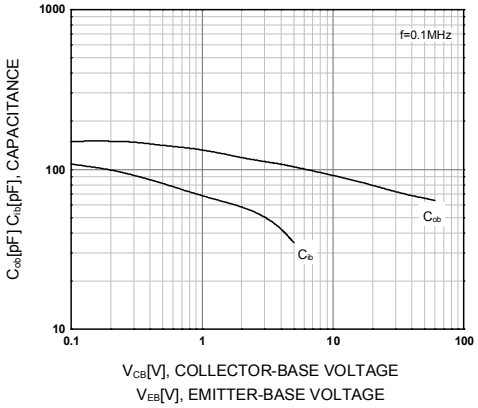

Figure 3. Output and Input Capacitance vs. Reverse Voltage

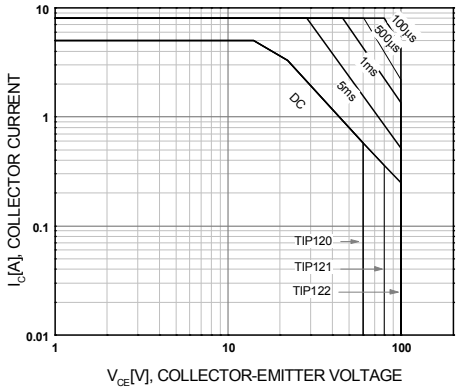

Figure 4. Safe Operating Area

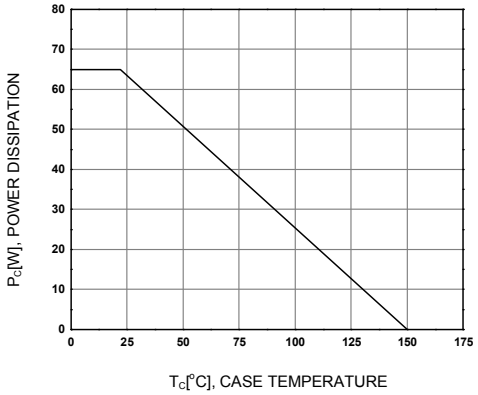

Figure 5. Power Derating

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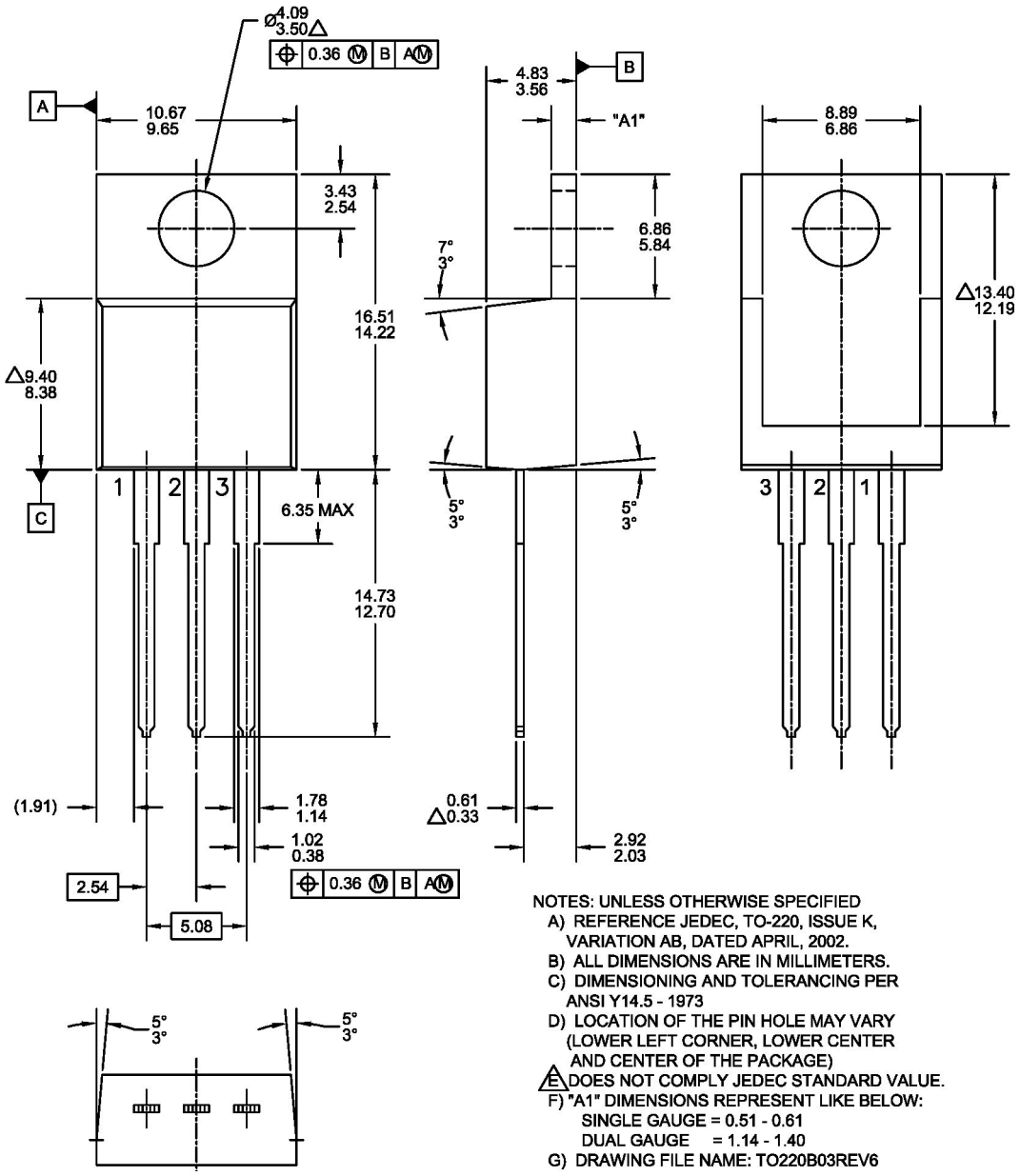
Mechanical Dimensions

TO220



NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.14 - 1.40
G) DRAWING FILE NAME: TO220B03REV6

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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