2V$_{RMS}$ DirectPath™, 112/106/100dB Audio Stereo DAC with 32-bit, 384kHz PCM Interface

Check for Samples: PCM5102-Q1

FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the following results:**
  - **Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **Market-Leading Low Out-of-Band Noise**
- **Selectable Digital-Filter Latency and Performance**
- **No DC Blocking Capacitors Required**
- **Integrated Negative Charge Pump**
- **Internal Pop-Free Control For Sample-Rate Changes Or Clock Halts**
- **Intelligent Muting System; Soft Up/Down Ramp and Analog Mute For 120dB Mute SNR With Popless Operation.**
- **Integrated High-Performance Audio PLL With BCK Reference To Generate SCK Internally**
- **Small 28-pin TSSOP Package**

Typical Performance (3.3V Power Supply)

Parameter	PCM5102 / PCM5101 / PCM5100
SNR	112 / 106 / 100dB
Dynamic Range	112 / 106 / 100dB
THD+N at - 1dBFS	–93 / –92 / –90dB
Full Scale Output	2.1V$_{RMS}$ (GND center)
Normal 8× Oversampling Digital Filter Latency: 20/f_S	
Low Latency 8× Oversampling Digital Filter Latency: 3.5/f_S	
Sampling Frequency	8kHz to 384kHz
System Clock Multiples (f_{SCK}): 64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz	

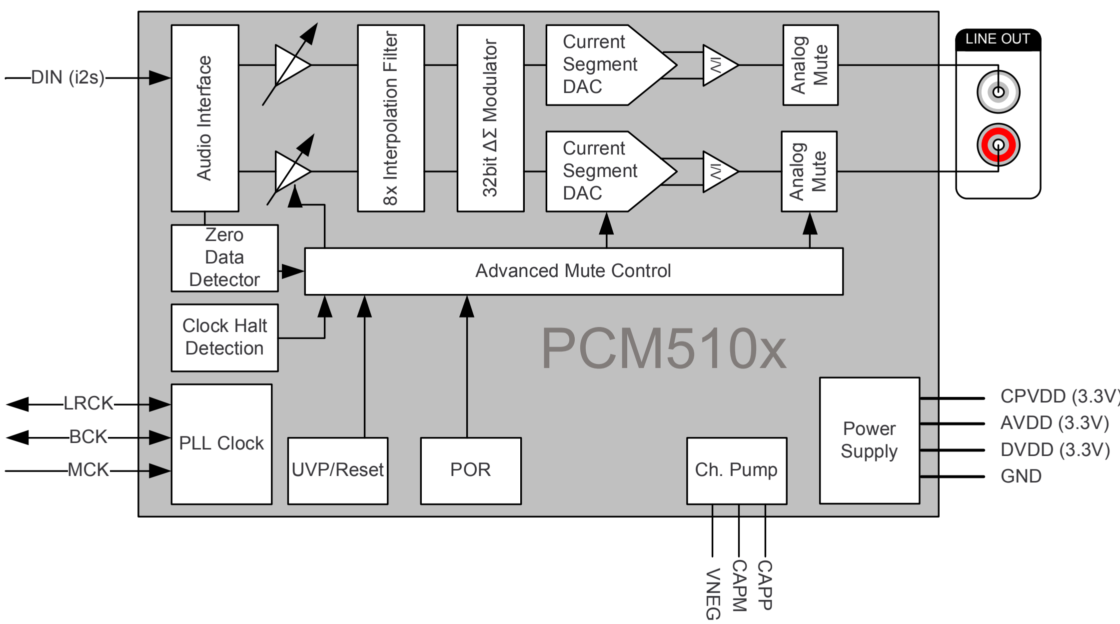


Figure 1. PCM5102-Q1 Functional Block Diagram

OTHER KEY FEATURES

- **Accepts 16-, 24-, And 32-Bit Audio Data**
- **PCM Data Formats: I^2S, Left-Justified**
- **Automatic Power-Save Mode When LRCK And BCK Are Deactivated.**
- **3.3V Failsafe LVCMOS Digital Inputs**
- **Hardware Configuration**
- **Single Supply Operation:**
  - **3.3V Analog, 3.3V Digital**
- **Integrated Power-On Reset**

APPLICATIONS

- **A/V Receivers**
- **DVD, BD Players**
- **HDTV Receivers**
- **Applications Requiring $2V_{RMS}$ Audio Output**

DESCRIPTION

The PCM5102-Q1 devices are a family of monolithic CMOS integrated circuits that include a stereo digital-to-analog converter and additional support circuitry in a small TSSOP package. The PCM5102-Q1 uses the latest generation of TI's advanced segment-DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter.

The PCM5102-Q1 provides $2.1V_{RMS}$ ground centered outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

The integrated line driver surpasses all other charge-pump based line drivers by supporting loads down to 1kΩ. By supporting loads down to 1kΩ, the PCM5102-Q1 can essentially drive up to 10 products in parallel. (LCD TV, DVDR, AV Receivers and so on).

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock). This allows a 3-wire I^2S connection, along with reduced system EMI.

Intelligent clock error and PowerSense under voltage protection utilizes a two level mute system for pop-free performance. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit

Compared with existing DAC technology, the PCM5102-Q1 family offers up to 20dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers/ADCs. (from traditional 100kHz OBN measurements all the way to 3MHz)

The PCM5102-Q1 accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384kHz are supported.

Table 1. Ordering Information

Part Number	T_A	Package	top_Side Symbool
PCM5102TPWRQ1	–40°C to 105°C	PW-TSSOP / Reel of 2000	PCM5102Q

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply Voltage	AVDD, CPVDD, DVDD	–0.3 to 3.9	V
Digital Input Voltage		–0.3 to 3.9	
Analog Input Voltage		–0.3 to 3.9	
Operating Temperature Range		–25 to 85	°C
Storage Temperature Range		–65 to 150	
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2	2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B	750	V

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Theta JA	High K		91.2		ºC/W
ψ_{JT}	Psi JT			1.0		
ψ_{JB}	Psi JB			41.5		
θ_{JC}	Theta JC	Top		25.3		
θ_{JB}	Theta JB			42.0		

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

Power Supply Requirements						
			MIN	NOM	MAX	UNIT
DV_{DD}	Digital supply voltage	Target DV_{DD} = 3.3V	3.0	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3.0	3.3	3.6	
CPV_{DD}	Charge-pump suply voltage		3.0	3.3	3.6	
I_{DD}	DV_{DD} supply current at 3.3V(1)	f_S = 48kHz		7	12	mA
		f_S = 96kHz		8		
		f_S = 192kHz		9		
I_{DD}	DV_{DD} supply current at 3.3V(2)	f_S = 48kHz		8	13	mA
		f_S = 96kHz		9		
		f_S = 192kHz		10		
I_{DD}	DV_{DD} supply current at 3.3V(3)			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(1)	f_S = 48kHz		11	16	mA
		f_S = 96kHz		11		
		f_S = 192kHz		11		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(2)	f_S = 48kHz		22	32	mA
		f_S = 96kHz		22		
		f_S = 192kHz		22		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current(3)	f_S = n/a		0.2	0.4	mA
	Power Dissipation, DV_{DD} = 3.3V(1)	f_S = 48kHz		59.4	92.4	mW
		f_S = 96kHz		62.7		
		f_S = 192kHz		66.0		
	Power Dissipation, DV_{DD} = 3.3V(2)	f_S = 48kHz		99.0	148.5	mW
		f_S = 96kHz		102.3		
		f_S = 192kHz		105.6		
	Power Dissipation, DV_{DD} = 3.3V(3)	f_S = n/a (Power Down Mode)		2.3	4.0	mW

(1) Input is Bipolar Zero data.
(2) Input is 1kHz -1dBFS data
(3) Power Down Mode

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		16	24	32	Bits
Data Format (PCM Mode)						
	Audio data interface format		I^2S, left justified			
	Audio data bit length		16, 24, 32-bit acceptable			
	Audio data format		MSB First, 2's Complement			
f_S	Sampling frequency		8		384	kHz
	System clock frequency		64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f_{SCK}, up to 50Mhz			
Digital Input/Output						
	Logic Family: 3.3V LVCMOS compatible					
V_{IH}	Input logic level		0.7×DV_{DD}			V
V_{IL}					0.3×DV_{DD}	
I_{IH}	Input logic current	V_{IN} = V_{DD}			10	µA
I_{IL}		V_{IN} = 0V			–10	
V_{OH}	Output logic level	I_{OH} = –4mA	0.8×DV_{DD}			V
V_{OL}		I_{OL} = 4mA			0.22×DV_{DD}	
Dynamic Performance (PCM Mode)(1)(2) (Values shown for three devices PCM5102/PCM5101/PCM5100)						
	THD+N at –1 dBFS(2)	f_S = 48kHz		–93/–92/–90	-83/ -82/ -80	dB
		f_S = 96kHz		–93/–92/–90		
		f_S = 192kHz		–93/–92/–90		
	Dynamic range(2)	EIAJ, A-weighted, f_S = 48kHz	106/ 100/ 95	112/106/100		
		EIAJ, A-weighted, f_S = 96kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192kHz		112/106/100		
	Signal-to-noise ratio(2)	EIAJ, A-weighted, f_S = 48kHz		112/106/100		
		EIAJ, A-weighted, f_S = 96kHz		112/106/100		
		EIAJ, A-weighted, f_S = 192kHz		112/106/100		
	Signal to noise ratio with analog mute(2)(3)	EIAJ, A-weighted, f_S = 48kHz	113	123		
		EIAJ, A-weighted, f_S = 96kHz		123		
		EIAJ, A-weighted, f_S = 192kHz		123		
	Channel Separation	f_S = 48 kHz	100/ 95/ 90	109/103/97		
		f_S = 96kHz		109/103/97		
		f_S = 192kHz		109/103/97		
Analog Output						
	Output voltage			2.1		V_{RMS}
	Gain error		–6	±2.0	6	% of FSR
	Gain mismatch, channel-to-channel		–6	±2.0	6	% of FSR
	Bipolar zero error	At bipolar zero	–5	±1.0	5	mV
	Load impedance		1			kΩ
Filter Characteristics–1: Normal						
	Pass band				0.45f_S	
	Stop band		0.55f_S			

(1) Filter condition: THD+N: 20Hz HPF, 20kHz AES17 LPF Dynamic range: 20Hz HPF, 20kHz AES17 LPF, A-weighted Signal-to-noise ratio: 20Hz HPF, 20kHz AES17 LPF, A-weighted Channel separation: 20Hz HPF, 20kHz AES17 LPF Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the RMS mode.
(2) Output load is 10kΩ, with 470Ω output resistor and a 2.2nF shunt capacitor (see recommended output filter).
(3) Assert XSMT or both L-ch and R-ch PCM data are BPZ

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Stop band attenuation		–60			dB
	Pass-band ripple				±0.02	dB
	Delay time			$20/f_S$		s
Filter Characteristics–2: Low Latency						
	Pass band				$0.47f_S$	
	Stop band		$0.55f_S$			
	Stop band attenuation		–52			dB
	Pass-band ripple				±0.0001	dB
	Delay time			$3.5/f_S$		s

DEVICE INFORMATION

TERMINAL FUNCTIONS, PCM5102-Q1

PCM5102-Q1 (top view)

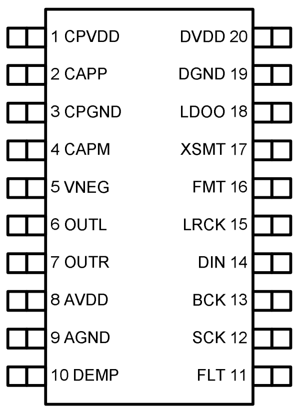


Table 2. PIN FUNCTIONS, PCM5102-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
CPVDD	1	—	Charge pump power supply, 3.3V
CAPP	2	O	Charge pump flying capacitor terminal for positive rail
CPGND	3	—	Charge pump ground
CAPM	4	O	Charge pump flying capacitor terminal for negative rail
VNEG	5	O	Negative charge pump rail terminal for decoupling, -3.3V
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
AVDD	8	-—	Analog power supply, 3.3V
AGND	9	—	Analog ground
DEMP	10	I	De-emphasis control for 44.1kHz sampling rate(1): Off (Low) / On (High)
FLT	11	I	Filter select : Normal latency (Low) / Low latency (High)
SCK	12	I	System clock input(1)
BCK	13	I	Audio data bit clock input(1)
DIN	14	I	Audio data input(1)

(1) Failsafe LVCMOS Schmitt trigger input

Table 2. PIN FUNCTIONS, PCM5102-Q1 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
LRCK	15	I	Audio data word clock input[1]
FMT	16	I	Audio format selection : I^2S (Low) / Left justified (High)
XSMT	17	I	Soft mute control[1]: Soft mute (Low) / soft un-mute (High)
LDOO	18	—	Internal logic supply rail terminal for decoupling
DGND	19	—	Digital ground
DVDD	20	—	Digital power supply, 3.3V

TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

PCM5100 THD+N vs Input Level

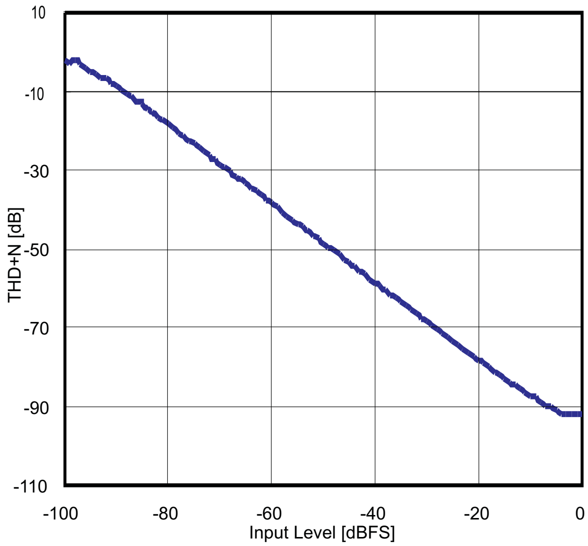


Figure 2.

PCM5101 THD+N vs Input Level

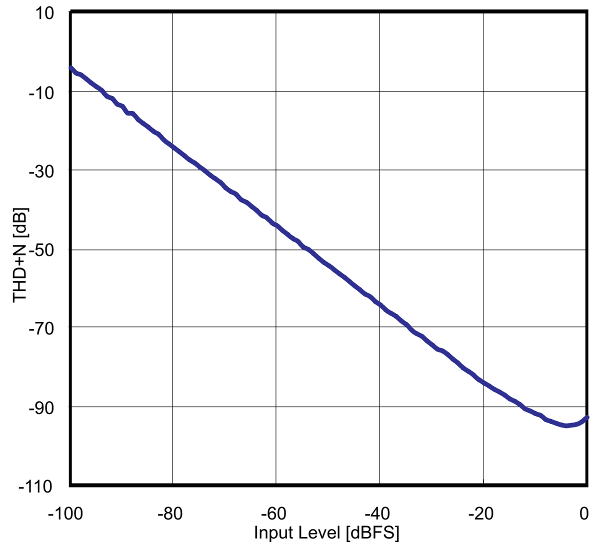


Figure 3.

PCM5102 THD+N vs Input Level

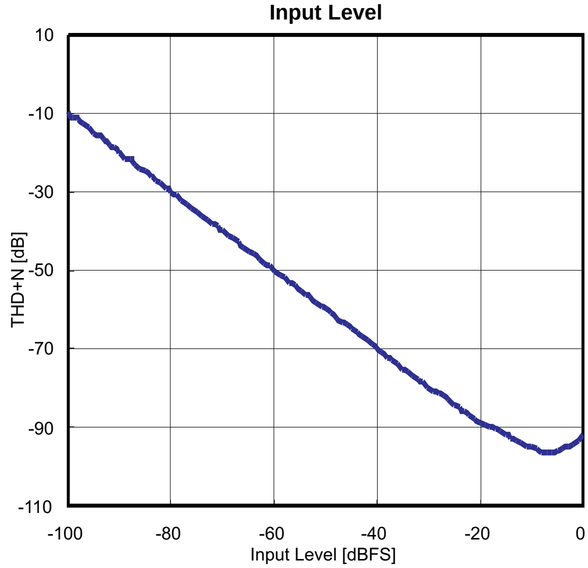


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

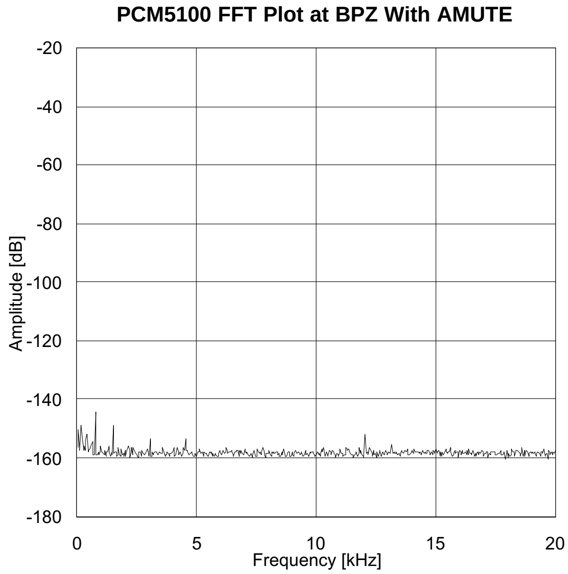


Figure 5.

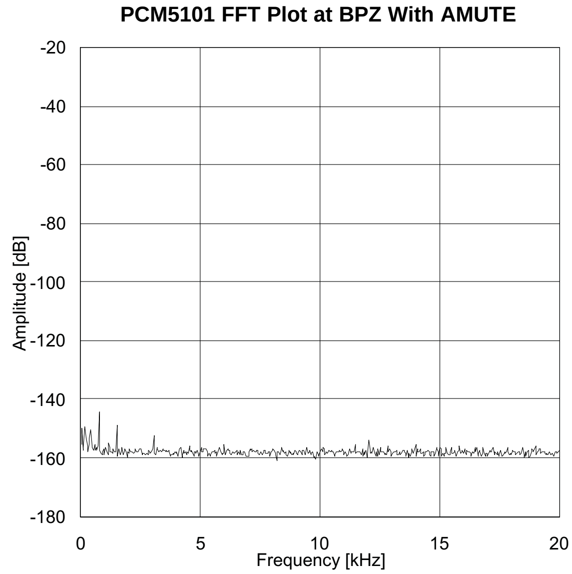


Figure 6.

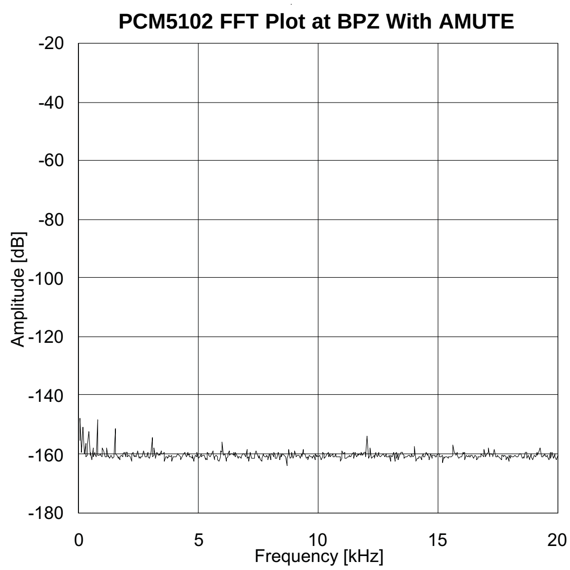


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AV_{DD} = CPV_{DD} = DV_{DD} = 3.3V, f_S = 48kHz, system clock = 512 f_S and 24-bit data unless otherwise noted.

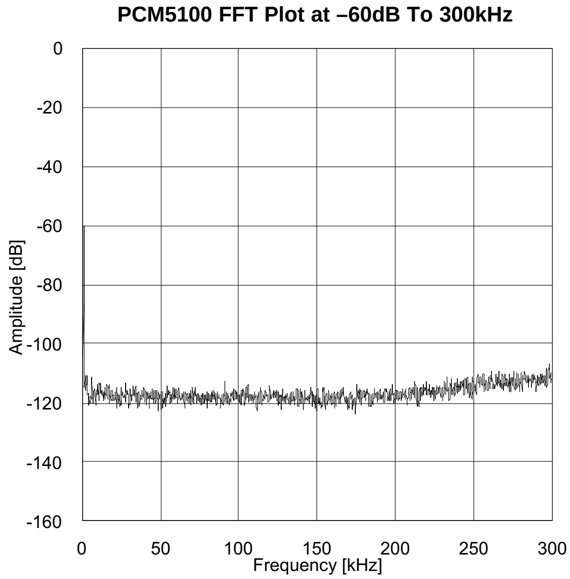


Figure 8.

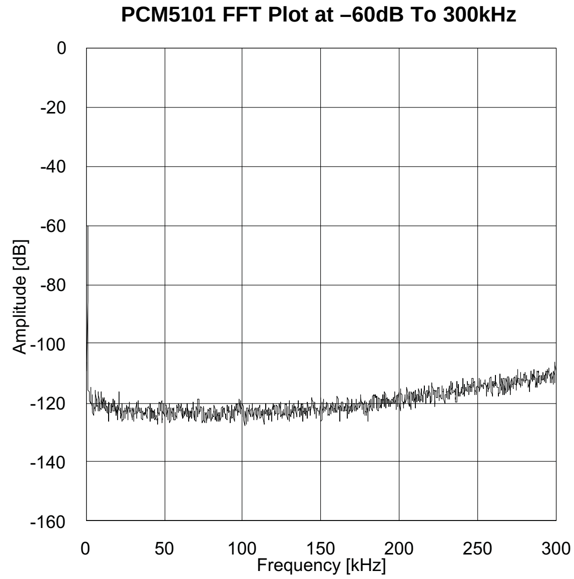


Figure 9.

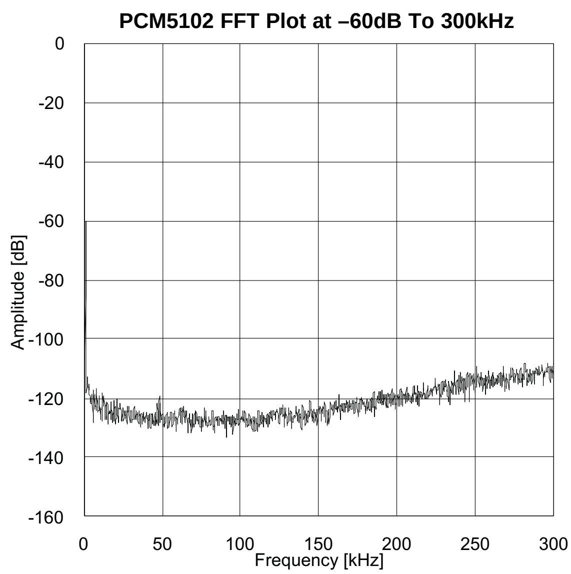


Figure 10.

APPLICATION INFORMATION

Reset and System Clock Functions

Power-On Reset Function

The PCM5102-Q1 includes a power-on reset function shown in Figure 11. With V_{DD} > 2.8V, the power-on reset function is enabled. After the initialization period, the PCM5102-Q1 is set to its default reset state.

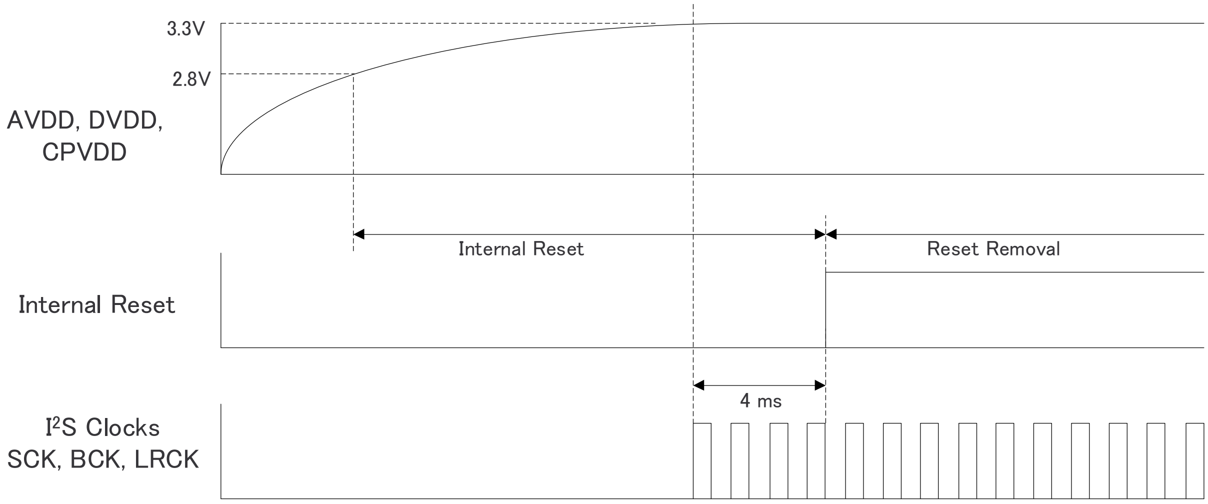


Figure 11. Power-On Reset Timing, DVDD = 3.3V

System Clock Input

The PCM5102-Q1 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 12) and supports up to 50MHz. The PCM5102-Q1 has a system-clock detection circuit that automatically senses the system-clock frequency. Common audio sampling frequencies of 8kHz, 16kHz, 32kHz - 44.1kHz - 48kHz, 88.2kHz - 96kHz, 176.4kHz - 192kHz, and 384kHz with ±4% tolerance are supported. The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge pump (NCP) automatically. Table 3 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1MHz and 50MHz, are only supported in software mode, available only in the PCM512x and PCM514x devices, by configuring various PLL and clock-divider registers. This allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (e.g. using 12MHz to generate 44.1kHz (LRCK) and 2.8224MHz (BCK)).

Figure 12 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise.

Table 3. System Master Clock Inputs for Audio Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	–[1]	1.0240[2]	1.5360[2]	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	–[1]	2.0480[2]	3.0720[2]	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	–[1]	4.0960[2]	6.1440[2]	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	–[1]	–[1]
44.1 kHz	–[1]	5.6488[2]	8.4672[2]	11.2896	16.9344	22.5792	33.8688	45.1584	–[1]	–[1]	–[1]	–[1]
48 kHz	–[1]	6.1440[2]	9.2160[2]	12.2880	18.4320	24.5760	36.8640	49.1520	–[1]	–[1]	–[1]	–[1]
88.2 kHz	–[1]	11.2896[2]	16.9344	22.5792	33.8688	45.1584	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]
96 kHz	–[1]	12.2880[2]	18.4320	24.5760	36.8640	49.1520	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]
176.4 kHz	–[1]	22.5792	33.8688	45.1584	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]
192 kHz	–[1]	24.5760	36.8640	49.1520	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]
384 kHz	24.5760	49.1520	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]	–[1]

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

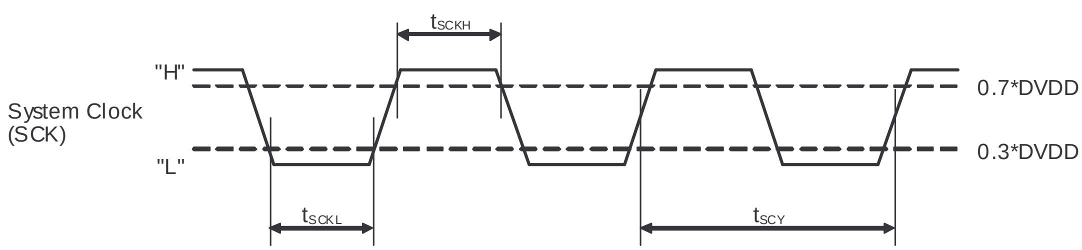


Figure 12. Timing Requirements for SCK Input

Table 4. Timing Requirements for SCK Input

	Parameters	Min	Max	Unit
t_{SCY}	System clock pulse cycle time	20	1000	ns
t_{SCKH}	System clock pulse width, High	9		ns
t_{SCKL}	System clock pulse width, Low	9		ns

System Clock PLL Mode

The system clock PLL mode allows designers to use a simple 3-wire I^2S audio source when driving the DAC. This reduces the need for a high frequency SCK, making PCB layout easier, and reduces high frequency electromagnetic interference.

The device starts up expecting an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL will start, automatically generating an internal SCK from the BCK reference. In the PCM5102-Q1, the internal PLL is disabled when an external SCK is supplied; specific BCK rates are required to generate an appropriate master clock. describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

Table 5. BCK Rates (MHz) by LRCK Sample Rate for PCM5102-Q1 PLL Operation

Sample f (kHz)	BCK (f_S)	
	32	64
8	-	-
16	-	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

Audio Data Interface

Audio Serial Interface

The audio interface port is a 3-wire serial port. It includes LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, and it is used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM5102-Q1 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

Table 6. PCM5102-Q1 Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f_S]	SCK RATE [x f_S]	BCK RATE [x f_S]
Hardware Control	I^2S/LJ	32, 24, 20, 16	Up to 192kHz	128 – 3072 (≤50MHz)	64, 48, 32
			384kHz	64, 128	64, 48, 32

The PCM5102-Q1 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than 4 LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and BCK is completed.

PCM Audio Data Formats and Timing

The PCM5102-Q1 supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected using the FMT (pin 16), Low for I^2S, and High for Left-justified.

All formats require binary 2s complement, MSB-first audio data. Figure 13 shows a detailed timing diagram for the serial audio interface.

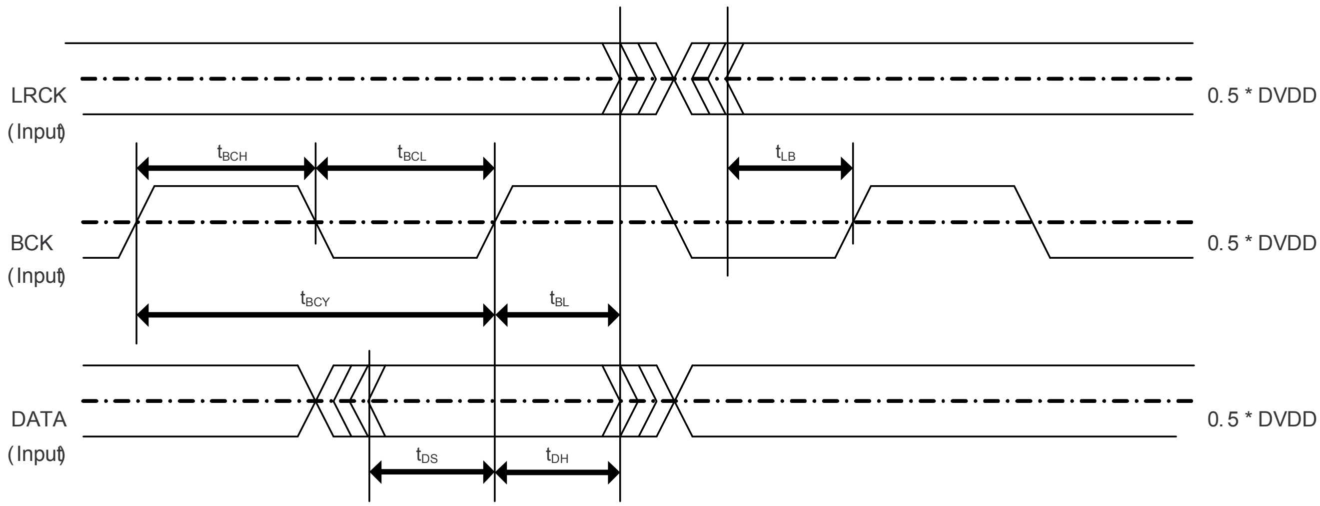


Figure 13. PCM5102-Q1 Serial Audio Timing - Slave

Table 7. Audio Interface Slave Timing

	Parameters	Min	Max	Units
t_{BCY}	BCK Pulse Cycle Time	40		ns
t_{BCL}	BCK Pulse Width LOW	16		ns
t_{BCH}	BCK Pulse Width HIGH	16		ns
t_{BL}	BCK Rising Edge to LRCK Edge	8		ns
t_{LB}	LRCK Edge to BCK Rising Edge	8		ns
t_{DS}	DATA Set Up Time	8		ns
t_{DH}	DATA Hold Time	8		ns
f_{BCK}	BCK frequency @ DVDD=3.3V		24.576	MHz

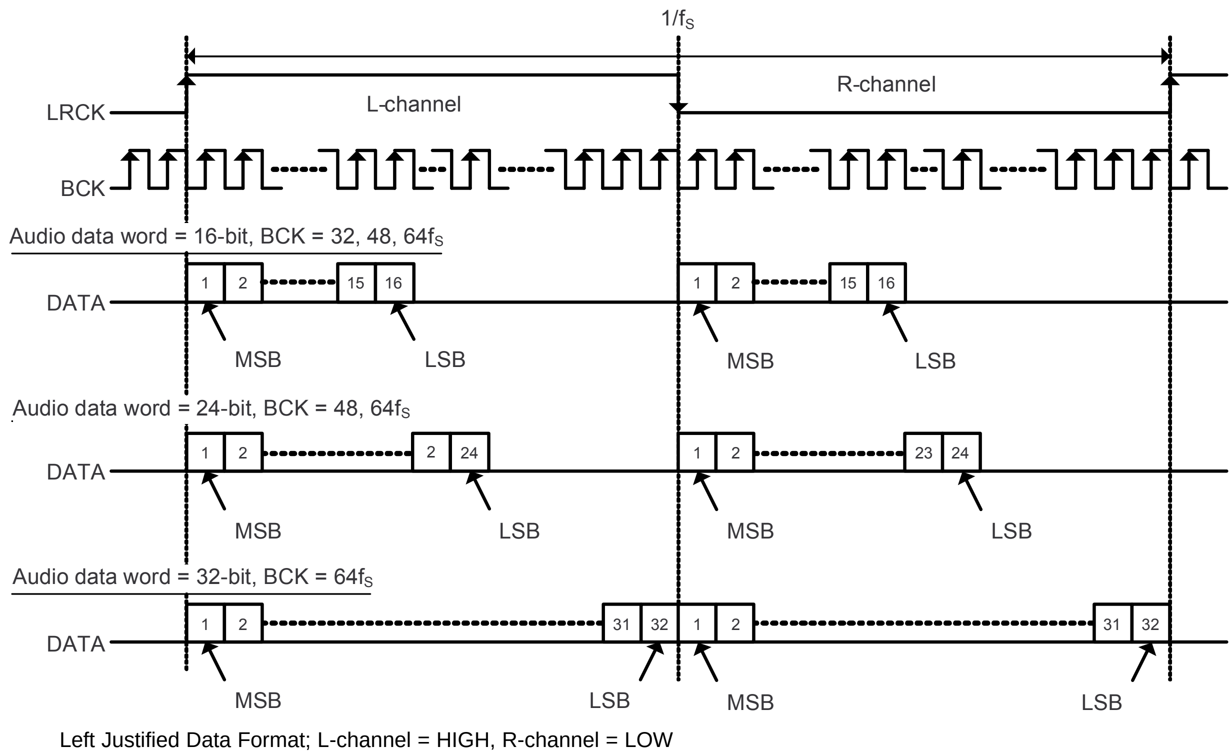


Figure 14. Left Justified Audio Data Format

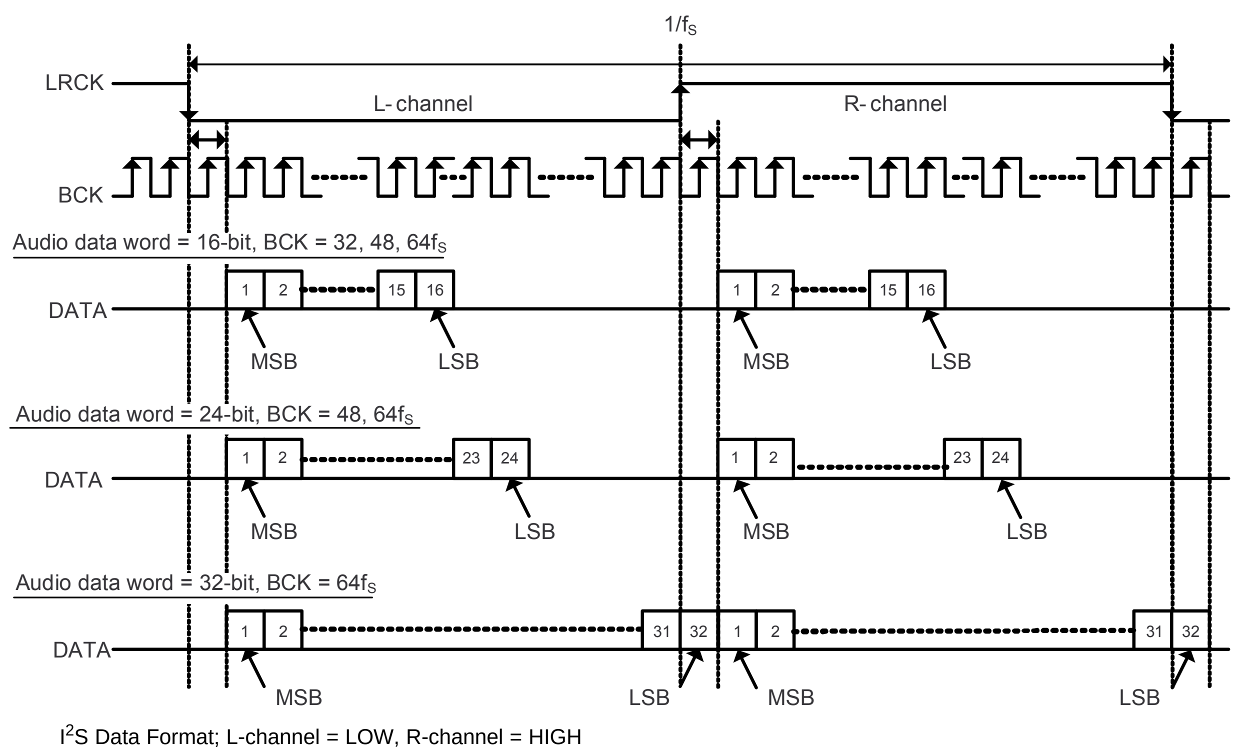


Figure 15. I²S Audio Data Format

Function Descriptions

Interpolation Filter

The PCM5102-Q1 provides 2 types of interpolation filter. Users can select which filter to use by using the FLT pin (pin11)

Table 8. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR Normal x8/x4/x2/x1 Interpolation Filters
1	IIR Low Latency x8/x4/x2/x1 Interpolation Filters

The Normal x8/x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) for from 8kHz to 384kHz.

Table 9. Normal x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. 0.45f_S		±0.02	dB
Filter Gain Stop Band	0.55f_S ….. 7.455f_S	–60		dB
Filter Group Delay		22/f_S		s

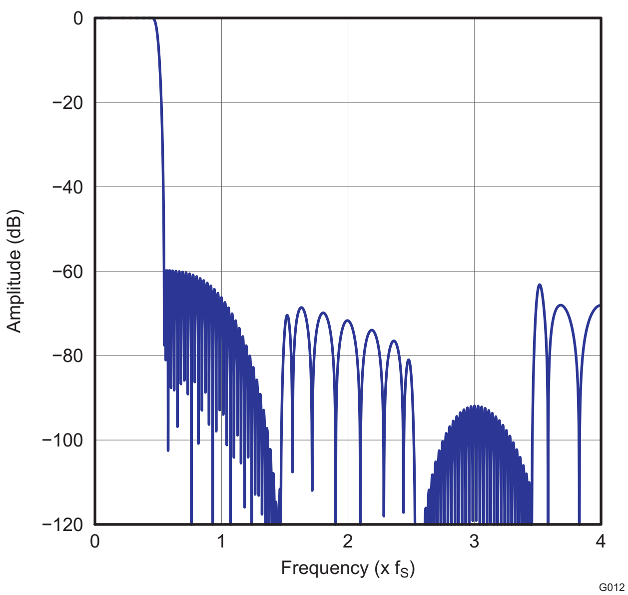


Figure 16. Normal x8 Interpolation Filter Frequency Response

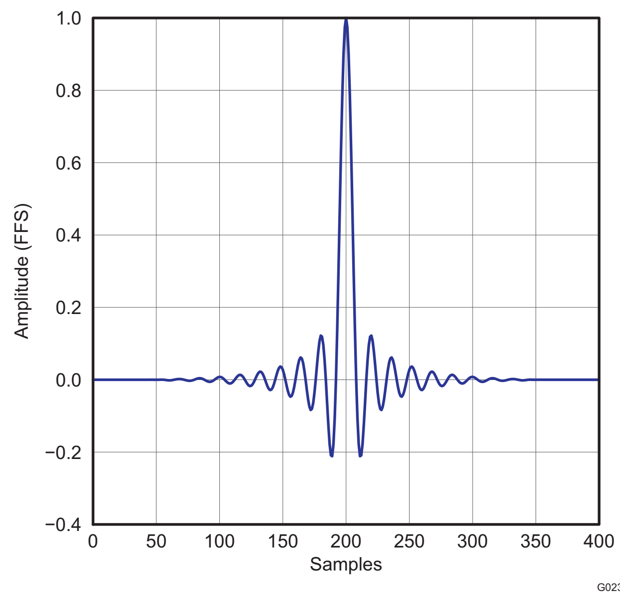


Figure 17. Normal x8 Interpolation Filter Impulse Response

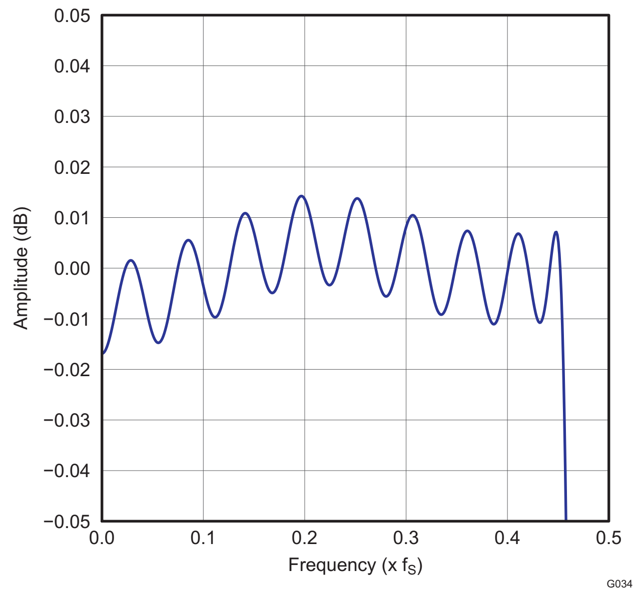


Figure 18. Normal x8 Interpolation Filter Passband Ripple

The Normal x4/x2/x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) for from 8kHz to 384kHz.

Table 10. Normal x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. 0.45f_S		±0.02	dB
Filter Gain Stop Band	0.55f_S ….. 7.455f_S	–60		dB
Filter Group Delay		22/f_S		s

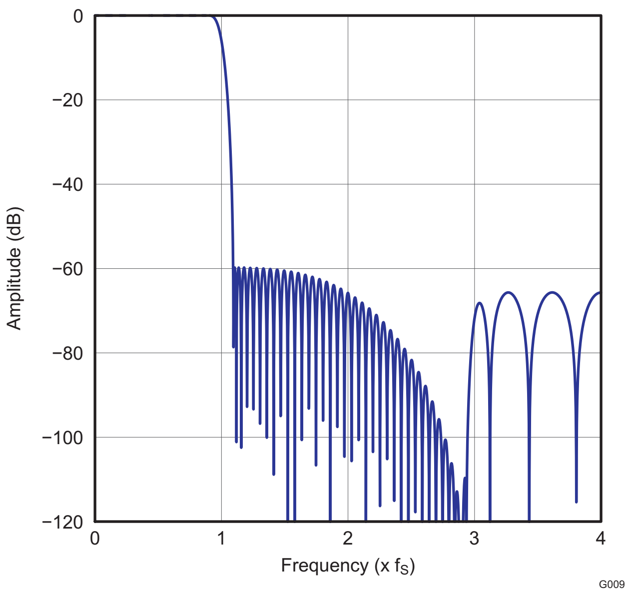


Figure 19. Normal x4 Interpolation Filter Frequency Response

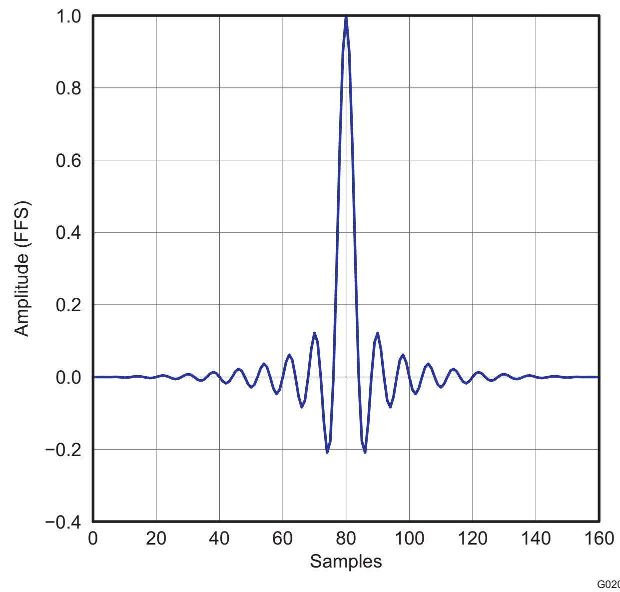


Figure 20. Normal x4 Interpolation Filter Impulse Response

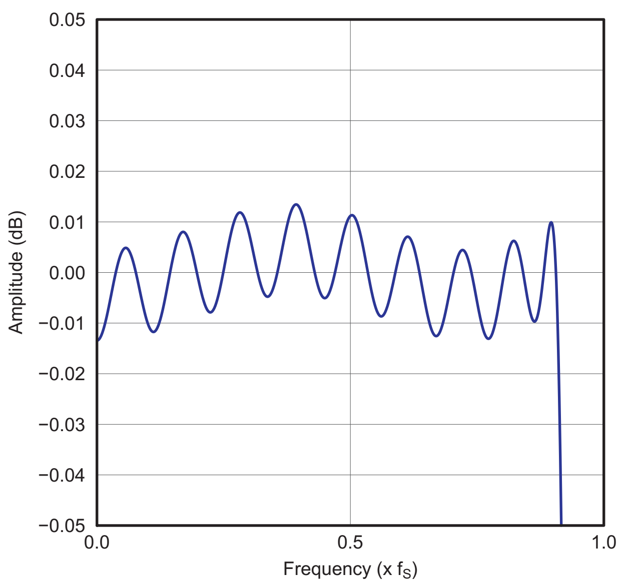


Figure 21. Normal x4 Interpolation Filter Passband Ripple

Normal x2 / x1(bypass) Interpolation filter is programmed in 256 cycles in 1 sampling frequency (f_S) for from 8kHz to 384kHz.

Table 11. Normal x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$		±0.02	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–60		dB
Filter Group Delay		$22/f_S$		s

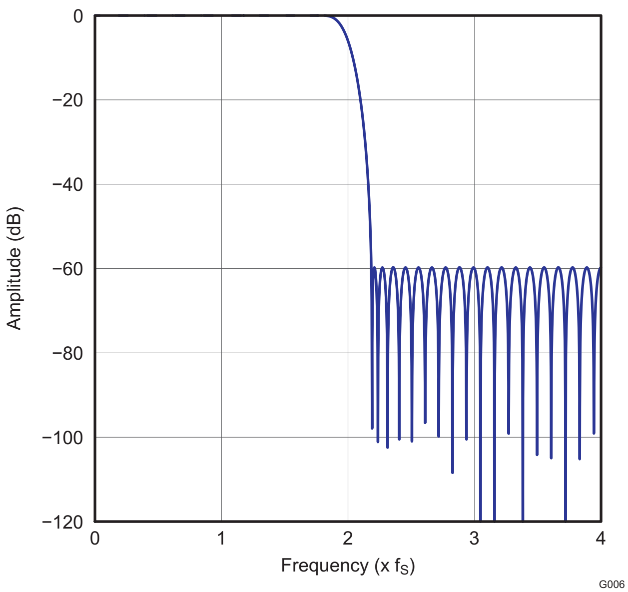


Figure 22. Normal x2 Interpolation Filter Frequency Response

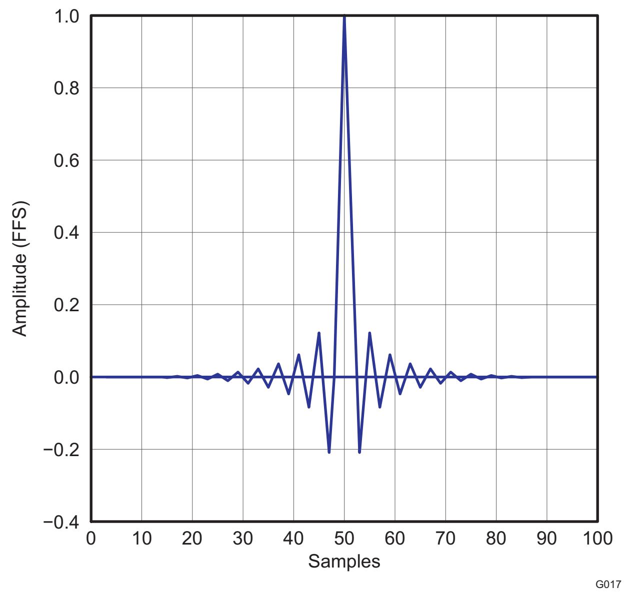


Figure 23. Normal x2 Interpolation Filter Impulse Response

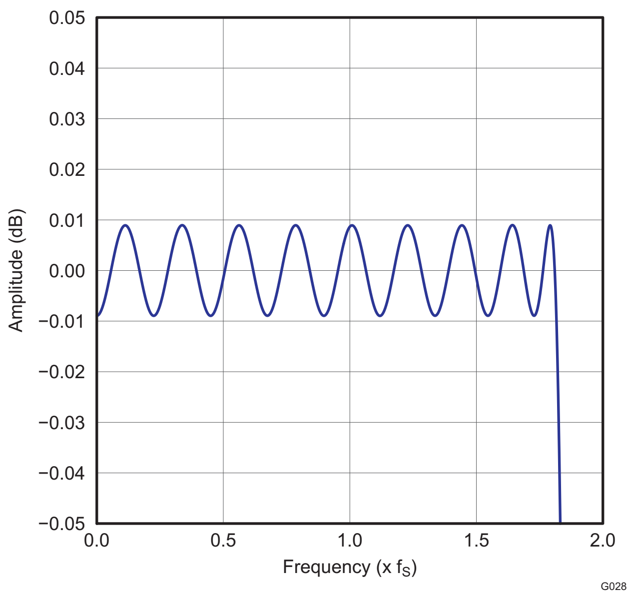


Figure 24. Normal x2 Interpolation Filter Passband Ripple

The low-latency x8 / x4 / x2 / x1(bypass) Interpolation filter is programmed in 256 cycles in $1f_S$ for from 8kHz to 384kHz.

Table 12. Low latency x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $7.455f_S$	–52	dB
Filter Group Delay		$3.5/f_S$	s

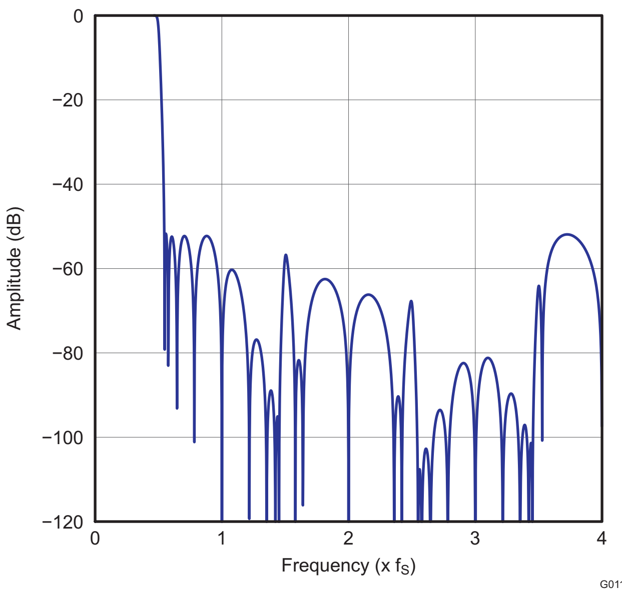


Figure 25. Low latency x8 Interpolation Filter Frequency Response

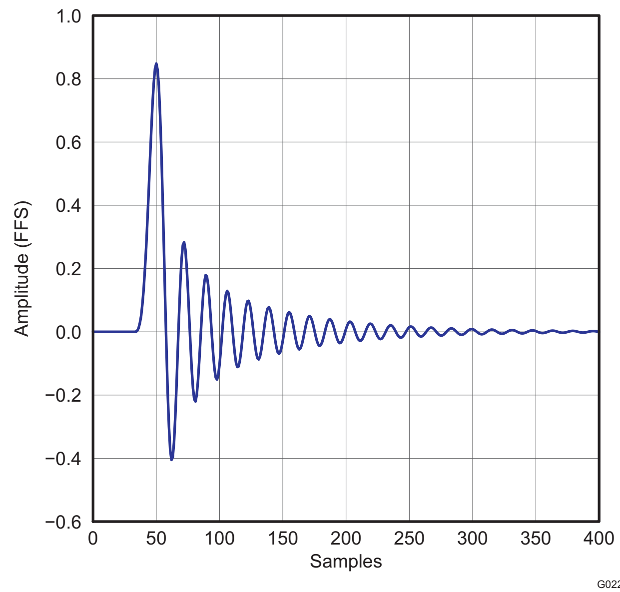


Figure 26. Low latency x8 Interpolation Filter Impulse Response

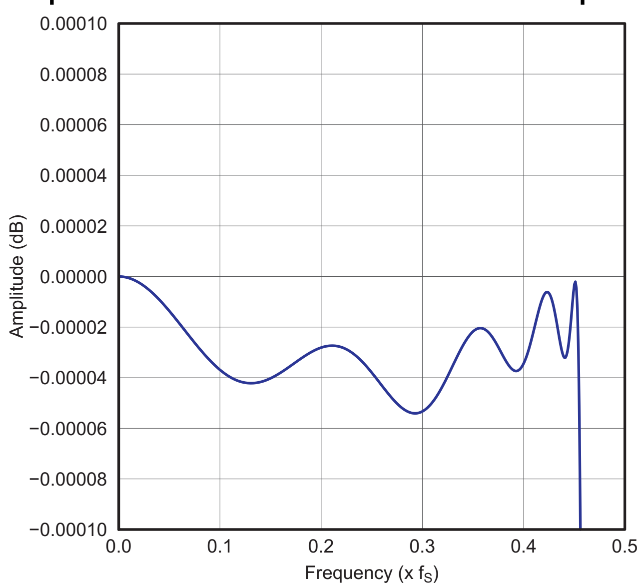


Figure 27. Low latency x8 Interpolation Filter Passband Ripple

Table 13. Low latency x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $3.455f_S$	–52	dB
Filter Group Delay		3.5	s

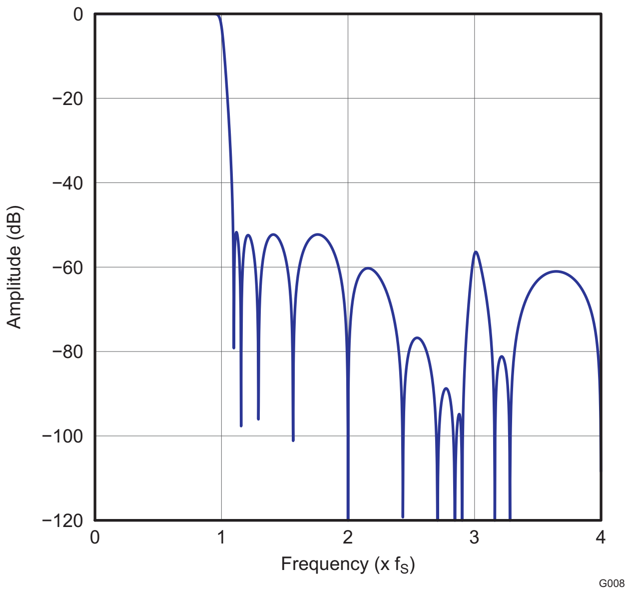


Figure 28. Low latency x4 Interpolation Filter Frequency Response

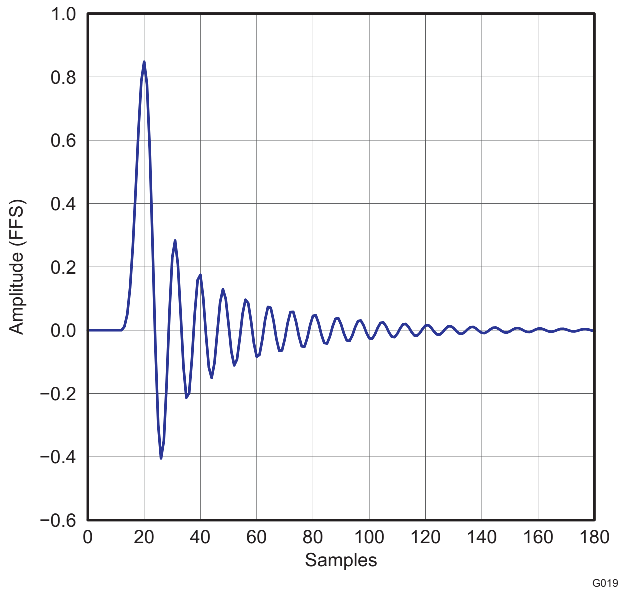


Figure 29. Low latency x4 Interpolation Filter Impulse Response

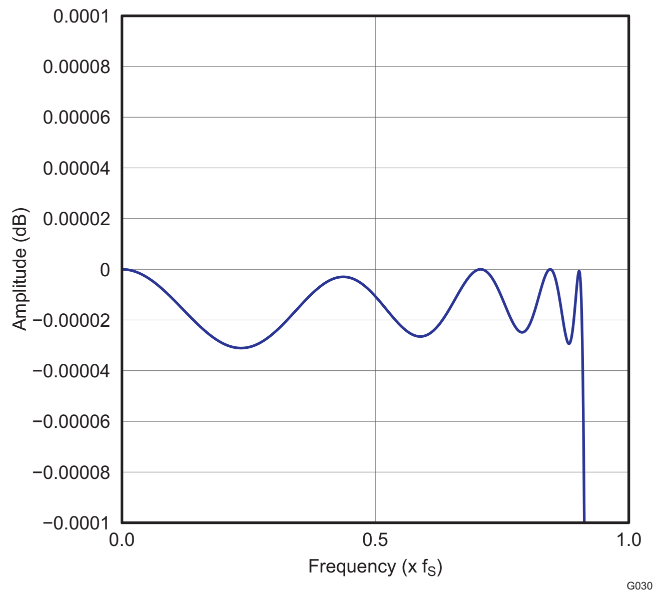


Figure 30. Low latency x4 Interpolation Filter Passband Ripple

Table 14. Low latency x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 ……. $0.45f_S$	±0.0001	dB
Filter Gain Stop Band	$0.55f_S$ ….. $1.455f_S$	–52	dB
Filter Group Delay		3.5	s

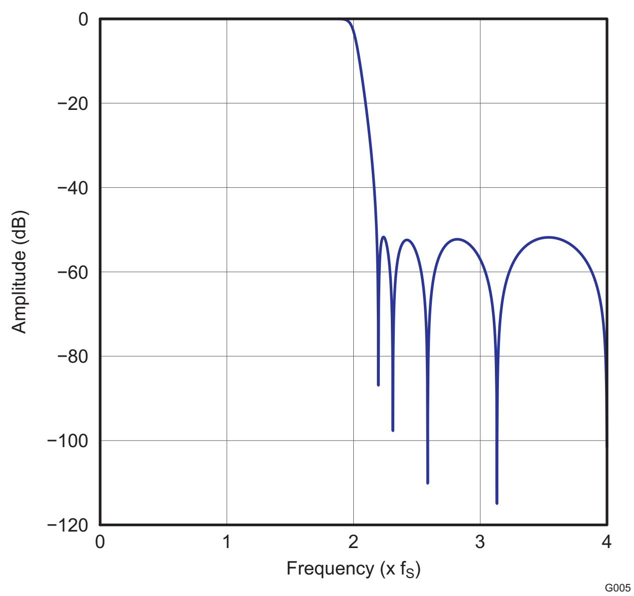


Figure 31. Low latency x2 Interpolation Filter Frequency Response

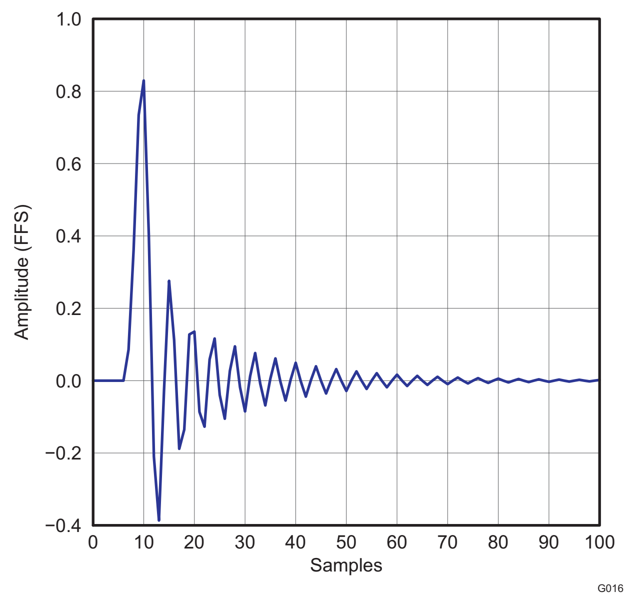


Figure 32. Low latency x2 Interpolation Filter Impulse Response

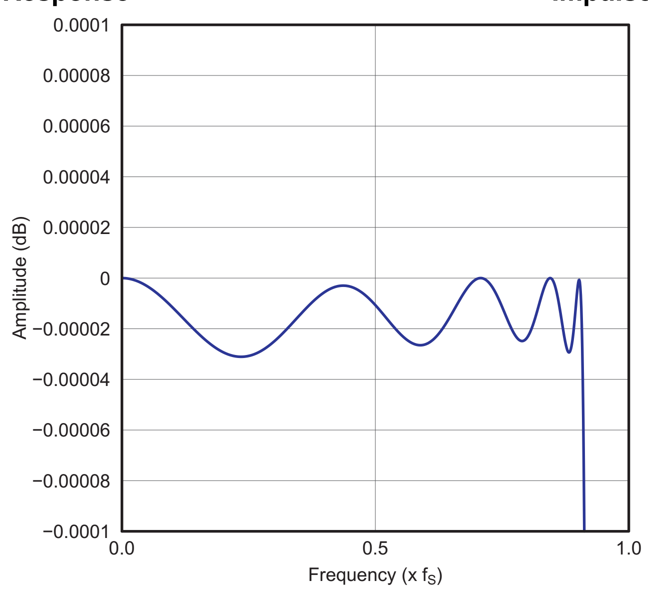


Figure 33. Low latency x2 Interpolation Filter Passband Ripple

Zero Data Detect

The PCM5102-Q1 has a zero-data detect function. When the device detects continuous zero data, it enters a full analog mute condition.

The PCM5102-Q1 counts zero data over 1024LRCKs (21ms @ 48kHz) before setting analog mute.

Power Save Mode

When any kind of clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM5102-Q1 enters Stand-by mode automatically. The current-segment DAC and Line driver are also powered down.

When BCK and LRCK halt to a low level for more than 1 second, the PCM5102-Q1 enters Power down mode automatically. Power-down mode includes the negative charge pump and Bias/Reference circuit power-down in addition to stand-by.

Whenever expected Audio clocks (SCK, BCK, LRCK) are applied to the PCM5102-Q1, the device starts its powerup sequence automatically.

XSMT Pin (Soft Mute / Soft Un-Mute)

For external digital control of the PCM5102-Q1, the XSMT pin must be driven by an external digital host with a specific/minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM5102-Q1 requires t_r/t_f times of less than 20ns. In the majority of applications, this shouldn't be a problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3V to 0V), a soft digital attenuation ramp is started. –1dB attenuation will be applied every $1f_S$ from 0dBFS to –∞. This takes 104 sample times.

When the XSMT pin is shifted from low to high (0V to 3.3V), a soft digital “un-mute” is started. 1dB gain steps are applied every f_S from –∞ to 0dBFS. This takes 104 sample times.

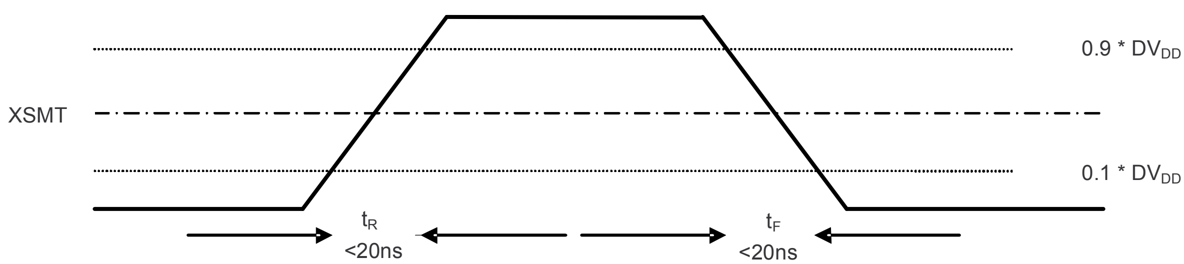


Figure 34. XSMT Timing for Soft Mute and Soft Un-Mute

Table 15. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time (t_R)		20	ns
Fall time (t_F)		20	ns

External Power Sense Undervoltage Protection mode

The XSMT pin can also be used to monitor a system voltage, such as the 24VDC LCD TV backlight, or 12VDC system supply using a potential divider created with two resistors. (See Figure 35)

- If the XSMT pin makes a transition from 1 to 0 over 6ms or more, the device will switch into external under-voltage protection mode. In this mode, two trigger levels are used.
- When XSMT pin level reaches 2V, soft mute process begins.
- When XSMT pin level reaches 1.2V, analog mute will engage, regardless of digital audio level, and analog shut down will begin. (i.e. DAC circuitry will power down etc).

A timing diagram to show this is shown in Figure 36.

NOTE

The XSMT input pins voltage range is from –0.3V to DVDD + 0.3V.The ratio of external resistors must be considered within this input range. Any increase in power supply (such as power supply positive noise/ripple) can pull the XSMT pin higher than DVDD+0.3V.

For example, if the PCM5102-Q1 is monitoring a 12V input, and dividing the voltage by 4, then the voltage at XSMT during ideal power supply conditions will be 3V. If the voltage spikes any higher than 14.4V, then XSMT will see a voltage in excess of 3.6V (DVDD+0.3), potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

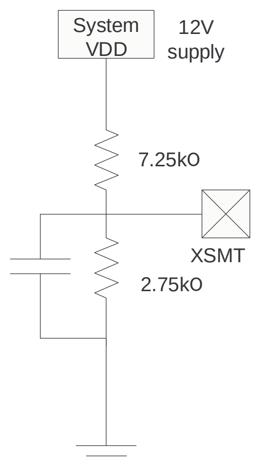


Figure 35. XSMT in External UVP Mode

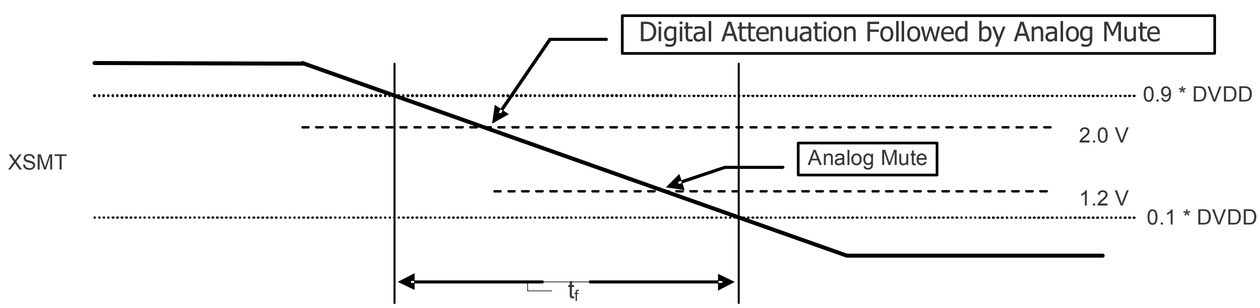


Figure 36. XSMT Timing for Undervoltage Protection

Typical Application Circuits

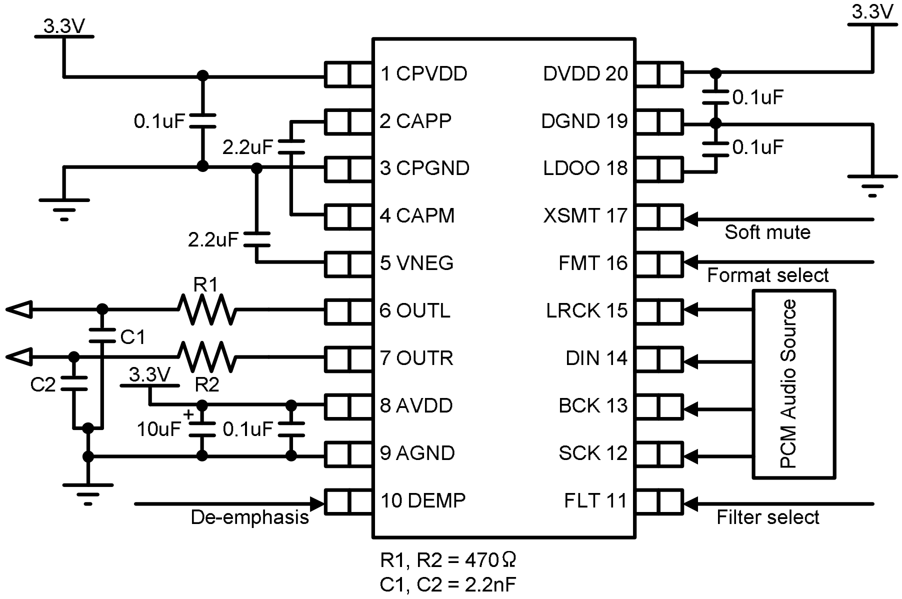


Figure 37. PCM5102-Q1 Standard PCM Audio Operation, 3.3V

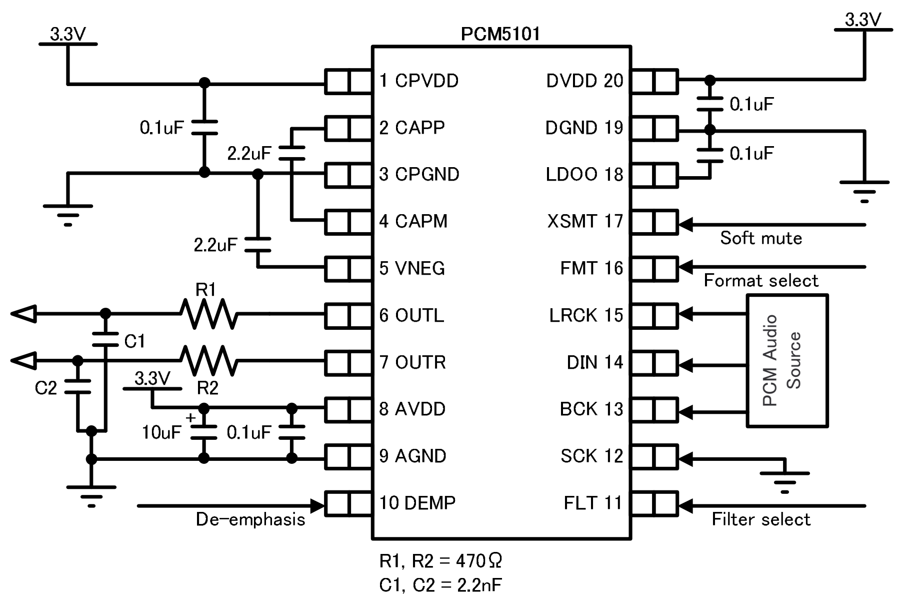


Figure 38. PCM5102-Q1 PLL Operation

Recommended Output Filter for the PCM5102-Q1

The diagram in Figure 39 shows the recommended output filter for the PCM5102-Q1. The new PCM5102-Q1 next generation current segment architecture offers excellent out of band noise, making a traditional 20kHz low pass filter a thing of the past.

The RC settings below offer a –3dB filter point at 153kHz (approx), giving the DAC the ability to reproduce virtually all frequencies through to it's maximum sampling rate of 384kHz.

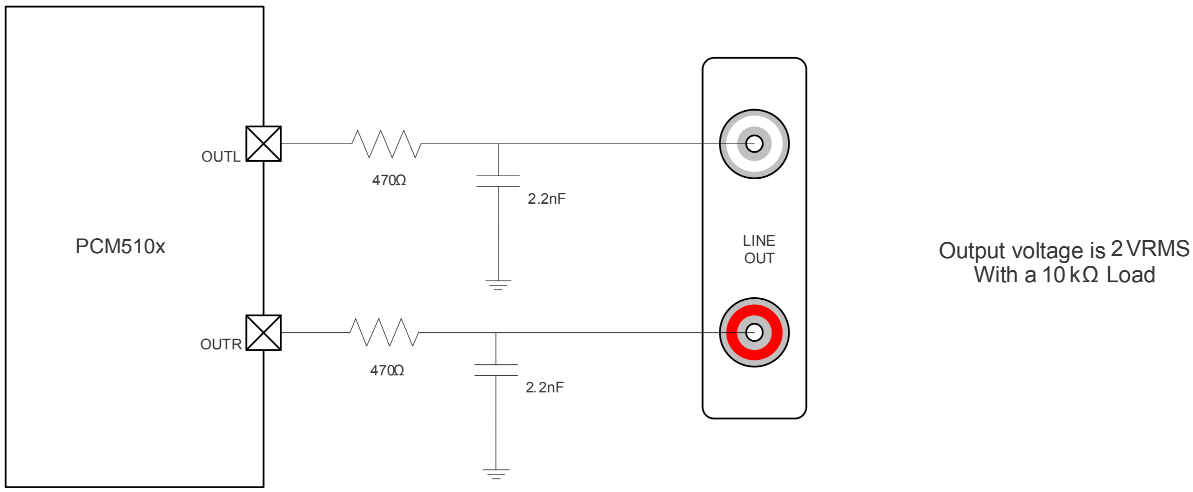


Figure 39. Recommended Output Lowpass Filter for 10kΩ Operation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
PCM5102TPWRQ1	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF PCM5102-Q1 :

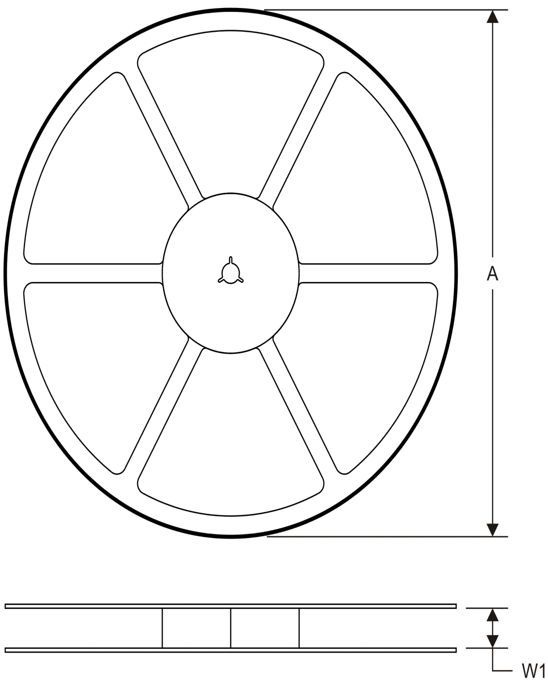
- Catalog: PCM5102

NOTE: Qualified Version Definitions:

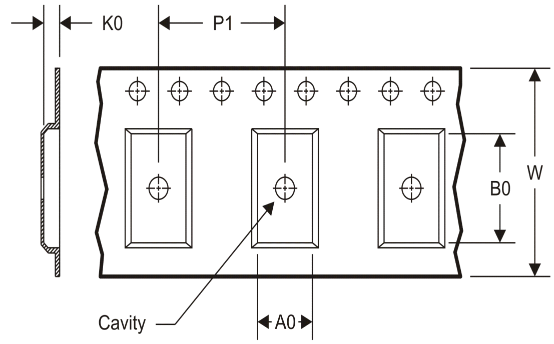
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



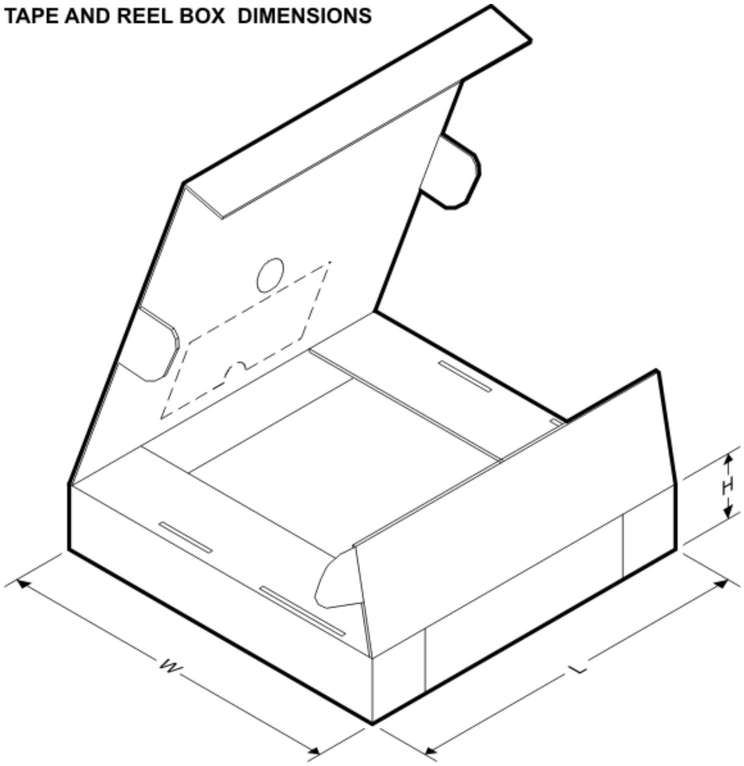
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5102TPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

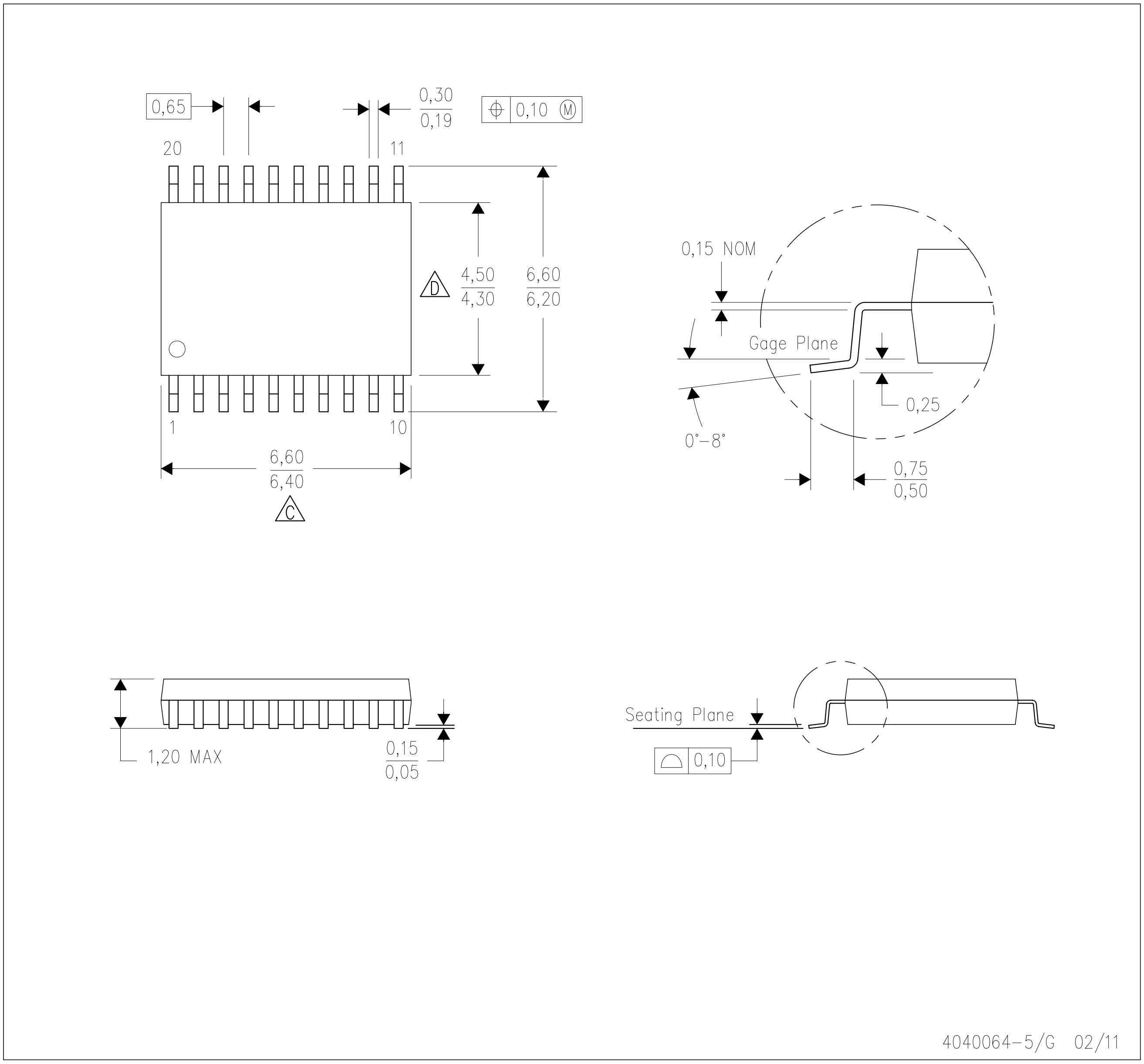
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

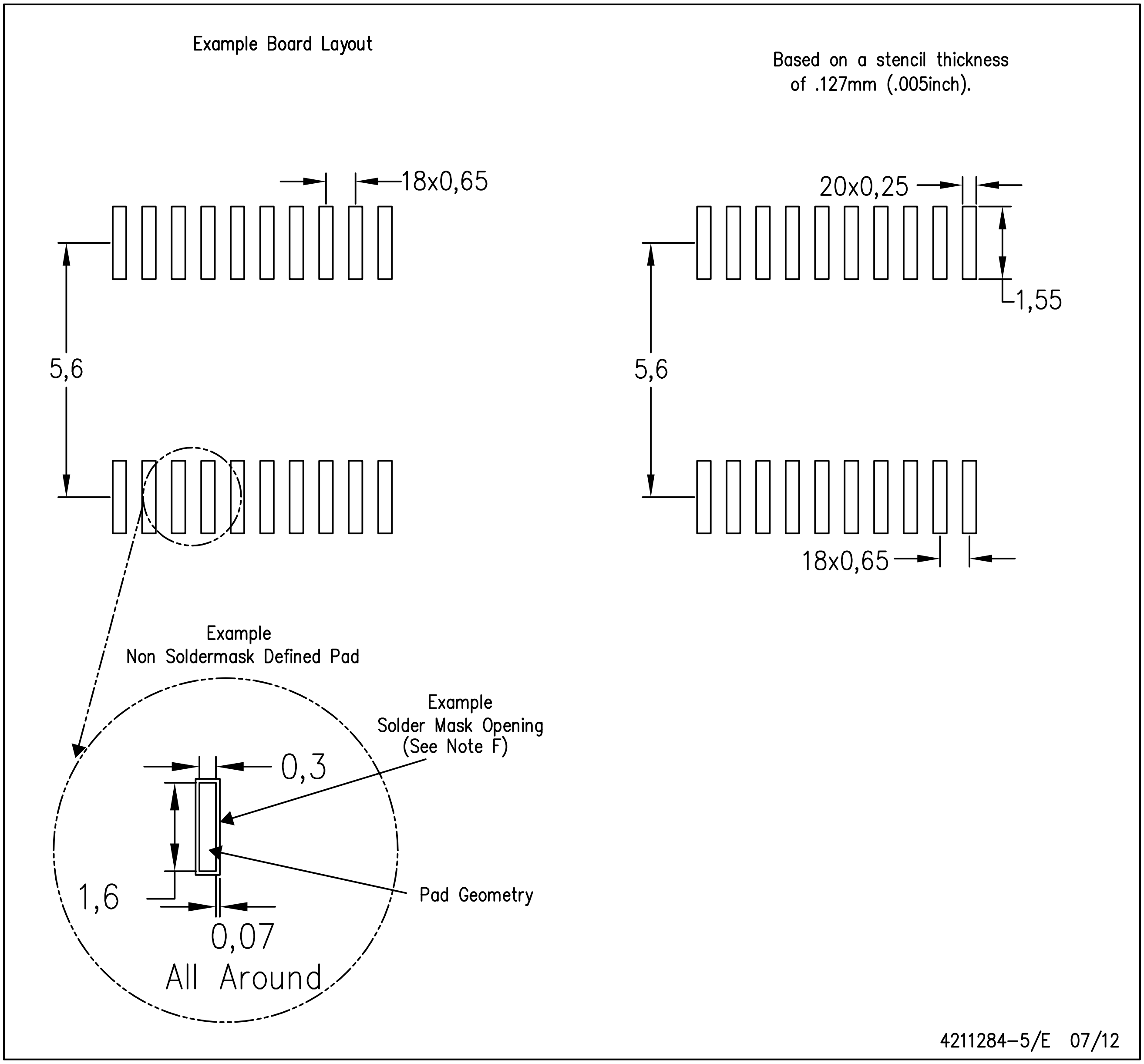
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5102TPWRQ1	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.