



# Dual-axis Magnetic Sensor, With I<sup>2</sup>C Interface

## MMC212xMG

### FEATURES

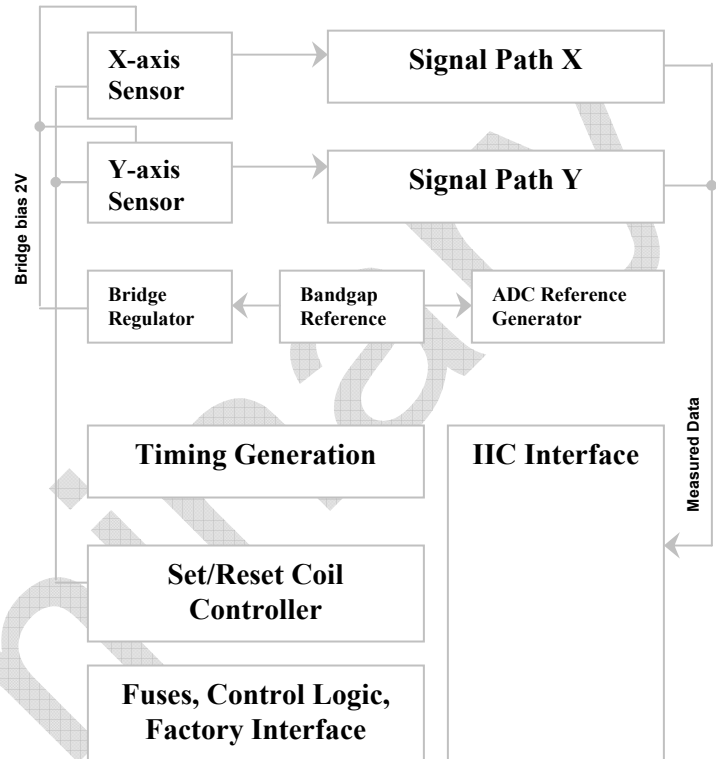
- Small Low profile package  
5.0x5.0x0.9mm
- Low power consumption: typically  
0.4mA@3V with 50 measurements per  
second
- RoHS compliant
- Full integration of 2-axis magnetic  
sensors and electronics circuits resulting  
in less external components needed.
- I<sup>2</sup>C Slave, FAST ( $\leq 400$  KHz) mode
- 1.8V compatible IO
- Power up/down function available through  
I<sup>2</sup>C interface
- 2.7V~5.25V wide power supply operation  
supported
- SET/RESET strap drive
- 512counts/gauss

### APPLICATIONS :

Electronic Compass  
GPS Navigation  
Position Sensing  
Vehicle Detection  
Magnetometry

### DESCRIPTIONS :

The MMC212xMG is a dual-axis magnetic sensor, it is a complete sensing system with on-chip signal processing and integrated I<sup>2</sup>C bus, allowing the device to be connected directly to a microprocessor eliminating the need for A/D converters or timing resources. It can measure magnetic field with a full range of  $\pm 2$  gauss and a sensitivity of 512counts/gauss @3.0 V at 25°C.



### FUNCTIONAL BLOCK DIAGRAM

The MMC212xMG is packaged in a small low profile LGA package (5.0x5.0x0.9mm) and is available in operating temperature ranges of -40°C to +85°C.

The MMC212xMG provides an I<sup>2</sup>C digital output with 400 KHz, fast mode operation.

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One Technology Drive, Suite 325, Andover, MA01810, USA  
Tel: +1 978 738 0900 Fax: +1 978 738 0196  
www.MEMSIC.com

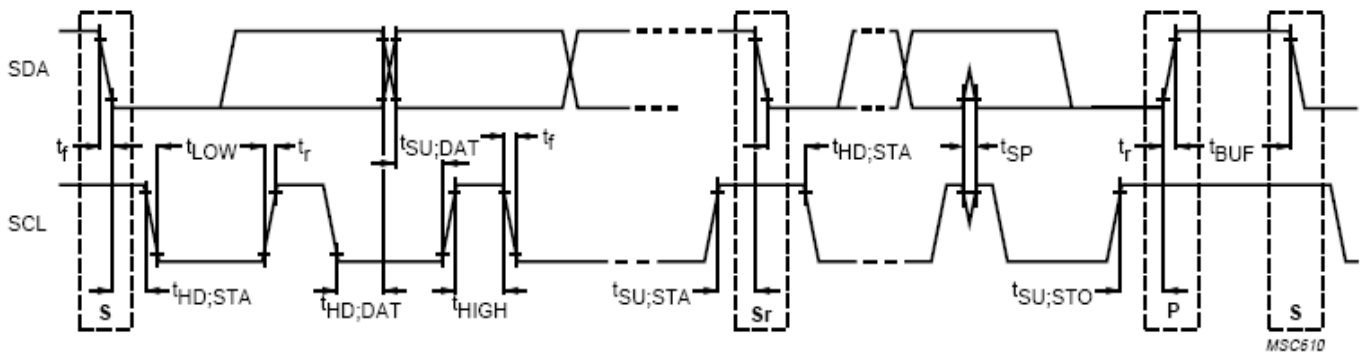
**SPECIFICATION:** (Measurements @ 25°C, unless otherwise noted;  $V_{DA} = V_{DD} = 3.0V$  unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Field Range (Each Axis)	Total applied field	-2		+2	gauss
Supply Voltage	$V_{DA}$	2.7	3.0	5.25	V
	$V_{DD}$ (I <sup>2</sup> C interface)	1.62	3.0	5.25	V
Supply Current	50 measurements/second		0.4		mA
Power Down Current				1.0	μA
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C
Linearity Error (Best fit straight line)	±1 gauss		0.1		%FS
	±2 gauss		0.5		%FS
Hysteresis	3 sweeps across ±2 gauss		0.05		%FS
Repeatability Error	3 sweeps across ±2 gauss		0.1		%FS
Alignment Error			±1.0	±3.0	degrees
Transverse Sensitivity			±2.0	±5.0	%
Noise Density	1~25Hz, RMS		600		μgauss
Accuracy <sup>1</sup>			±2	±5	deg
Bandwidth			25		Hz
Sensitivity		-10		+10	%
		461	512	563	counts/gauss
Sensitivity Change Over Temperature			±1100		ppm/°C
Null Field Output		-0.2		+0.2	gauss
			2048		counts
Null Field Output Change Over Temperature <sup>2</sup>	Without Set/Reset		±0.4		mgauss/°C
	With Set/Reset		1/50		Ratio to the result without set/reset
Disturbing Field	Sensitivity start to degrade, use Set/Reset pulse to restore	5.5			gauss
Maximum Exposed Field				10000	gauss

Note: <sup>1</sup>: Accuracy is dependent on system design, calibration and compensation algorithms used.  
The specification is based upon using the MEMSIC evaluation board and associate software.  
<sup>2</sup>: By design.

**I<sup>2</sup>C INTERFACE I/O CHARACTERISTICS (V<sub>DD</sub>=3.0V)**

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Logic Input Low Level	V <sub>IL</sub>		-0.5		0.3* V <sub>DD</sub>	V
Logic Input High Level	V <sub>IH</sub>		0.7*V <sub>DD</sub>		V <sub>DD</sub>	V
Hysteresis of Schmitt input	V <sub>hys</sub>		0.2			V
Logic Output Low Level	V <sub>OL</sub>				0.4	V
Input Leakage Current	I <sub>i</sub>	0.1V <sub>DD</sub> <V <sub>in</sub> <0.9V <sub>DD</sub>	-10		10	μA
SCL Clock Frequency	f <sub>SCL</sub>		0		400	kHz
START Hold Time	t <sub>HD;STA</sub>		0.6			μS
START Setup Time	t <sub>SU;STA</sub>		0.6			μS
LOW period of SCL	t <sub>LOW</sub>		1.3			μS
HIGH period of SCL	t <sub>HIGH</sub>		0.6			μS
Data Hold Time	t <sub>HD;DAT</sub>		0		0.9	μS
Data Setup Time	t <sub>SU;DAT</sub>		0.1			μS
Rise Time	t <sub>r</sub>	From V <sub>IL</sub> to V <sub>IH</sub>			0.3	μS
Fall Time	t <sub>f</sub>	From V <sub>IH</sub> to V <sub>IL</sub>			0.3	μS
Bus Free Time Between STOP and START	t <sub>BUF</sub>		1.3			μS
STOP Setup Time	t <sub>SU;STO</sub>		0.6			μS

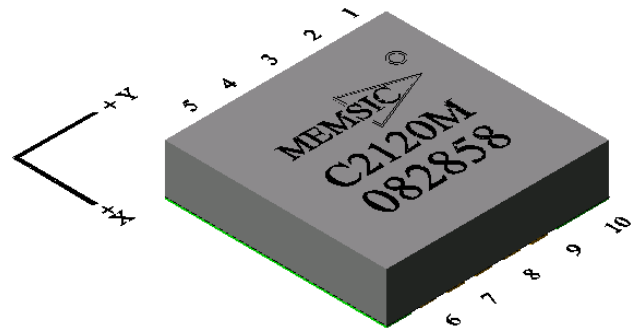


**Timing Definition**

**ABSOLUTE MAXIMUM RATINGS\***

Supply Voltage (V<sub>DA</sub>) .....-0.5 to +7.0V  
 Storage Temperature .....-55°C to +125°C  
 Maximum Exposed Field .....10000 gauss

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



The MEMSIC logo's arrow indicates the +Y sensing direction of the device.  
 Small circle indicates pin one (1).

**Pin Description: LGA-10 (5x5x0.9mm) Package**

Pin	Name	Description	I/O
1	TEST	Factory Use Only, Leave Open/No Connect	NC
2	CAP	Connect to External Capacitor	I
3	V <sub>DA</sub>	Power Supply	P
4	C+	Connect to External Capacitor	I
5	C-		I
6	GND	Connect to Ground	P
7	V <sub>DD</sub>	Power Supply for I <sup>2</sup> C bus	I
8	FM	Factory Use Only, Leave Open/No Connect, Internally Pulled Down	NC
9	SCL	Serial Clock Line for I <sup>2</sup> C bus	I
10	SDA	Serial Data Line for I <sup>2</sup> C bus	I/O

All parts are shipped in tape and reel packaging with 5000pcs per 13" reel.

**Caution:** ESD (electrostatic discharge) sensitive device.

**Ordering Guide:**

MMC212xMG

Package type:

Code	Type
G	LGA10 (5x5x0.9mm) RoHS compliant

Performance Grade:

Code	Temp
M	Low voltage operation mode, compensated

Address code: 0~3

Number	Address
0	60H
1	64H
2	68H
3	6CH

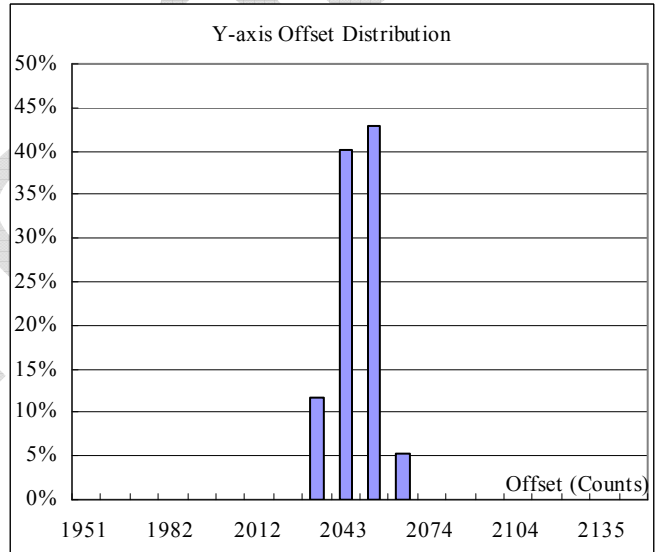
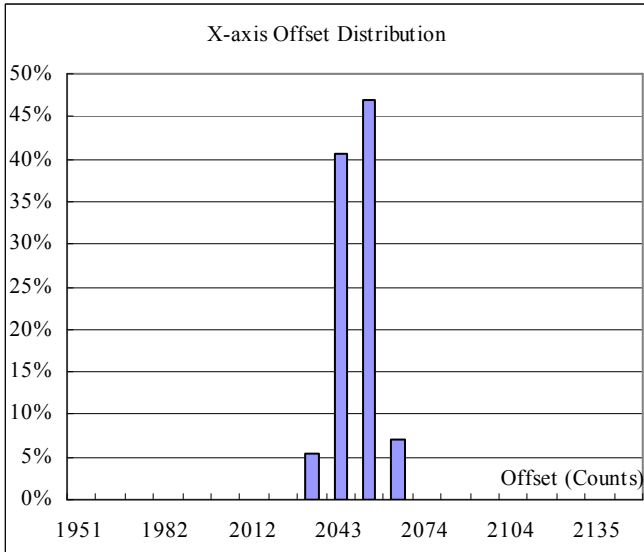
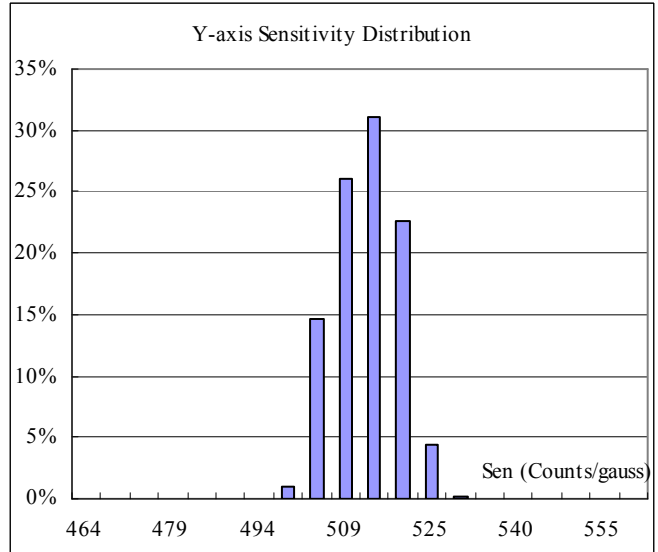
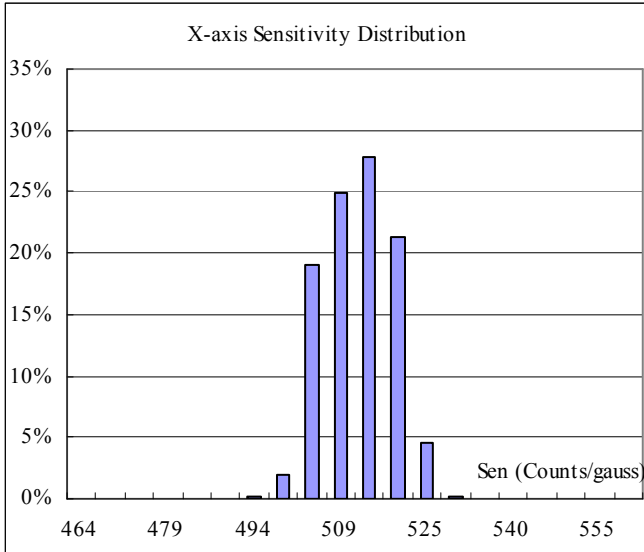
**THEORY:**

The anisotropic magnetoresistive (AMR) sensors are special resistors made of permalloy thin film deposited on a silicon wafer. During manufacturing, a strong magnetic field is applied to the film to orient its magnetic domains in the same direction, establishing a magnetization vector. Subsequently, an external magnetic field applied perpendicularly to the sides of the film causes the magnetization to rotate and change angle. This in turn causes the film's resistance to vary. The MEMSIC AMR sensor is included in a Wheatstone bridge, so that the change in resistance is detected as a change in differential voltage and the strength of the applied magnetic field may be inferred.

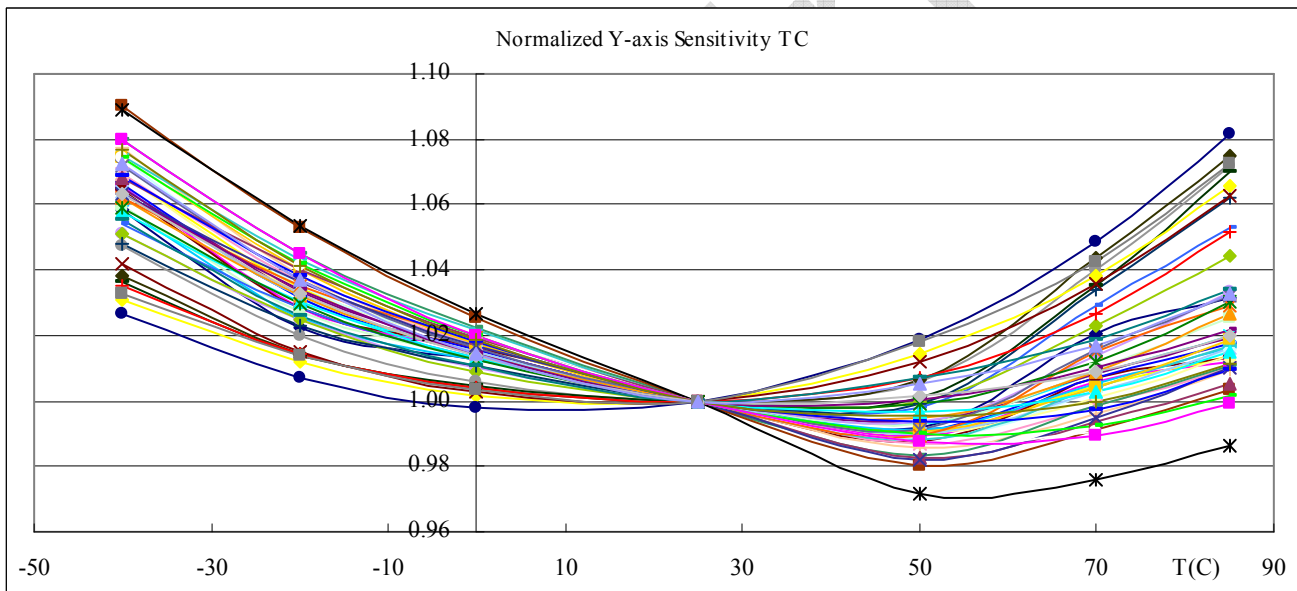
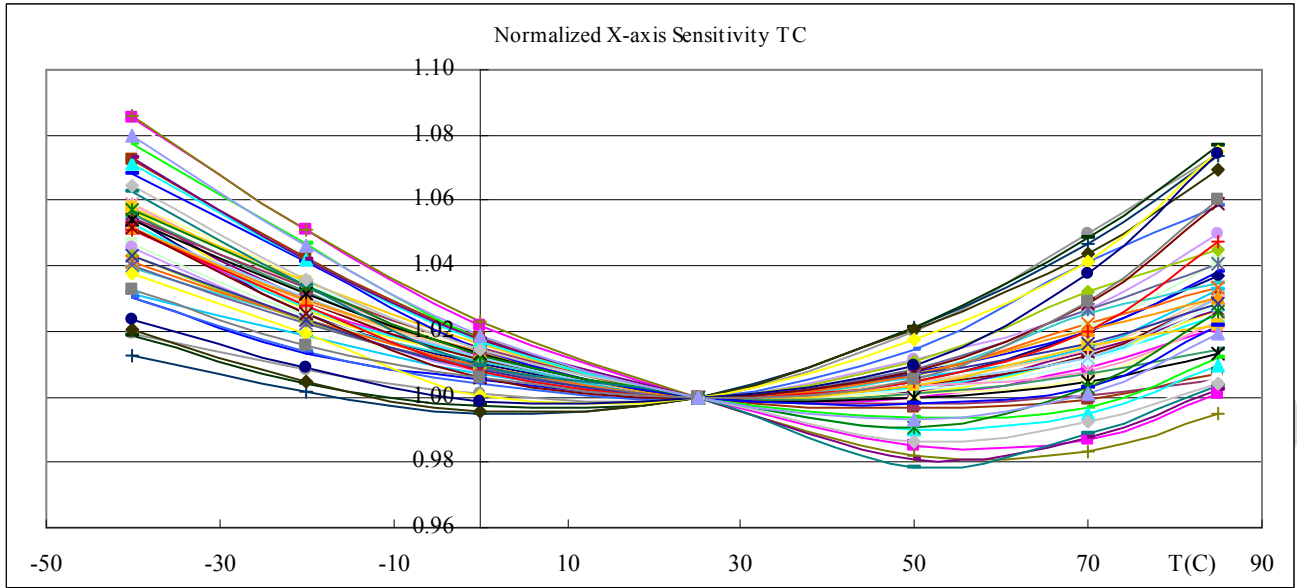
However, the influence of a strong magnetic field (more than 5.5 gauss) along the magnetization axis could upset, or flip, the polarity of the film, thus changing the sensor characteristics. A strong restoring magnetic field must be applied momentarily to restore, or set, the sensor characteristics. The MEMSIC magnetic sensor has an on-chip magnetically coupled strap: a SET/RESET strap pulsed with a high current, to provide the restoring magnetic field.

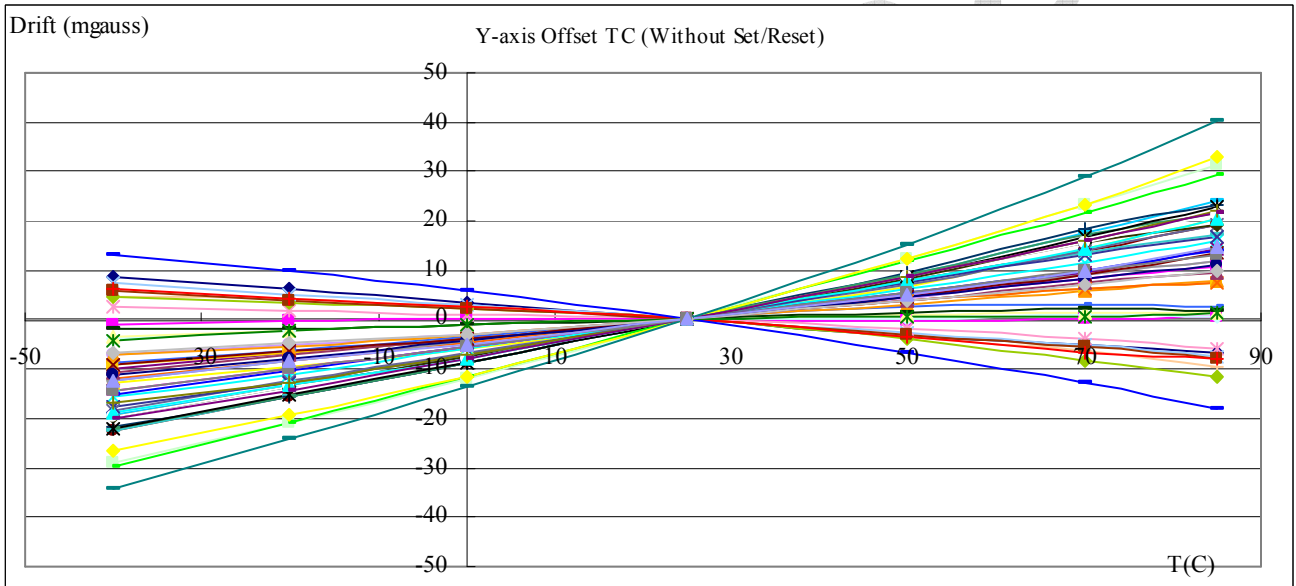
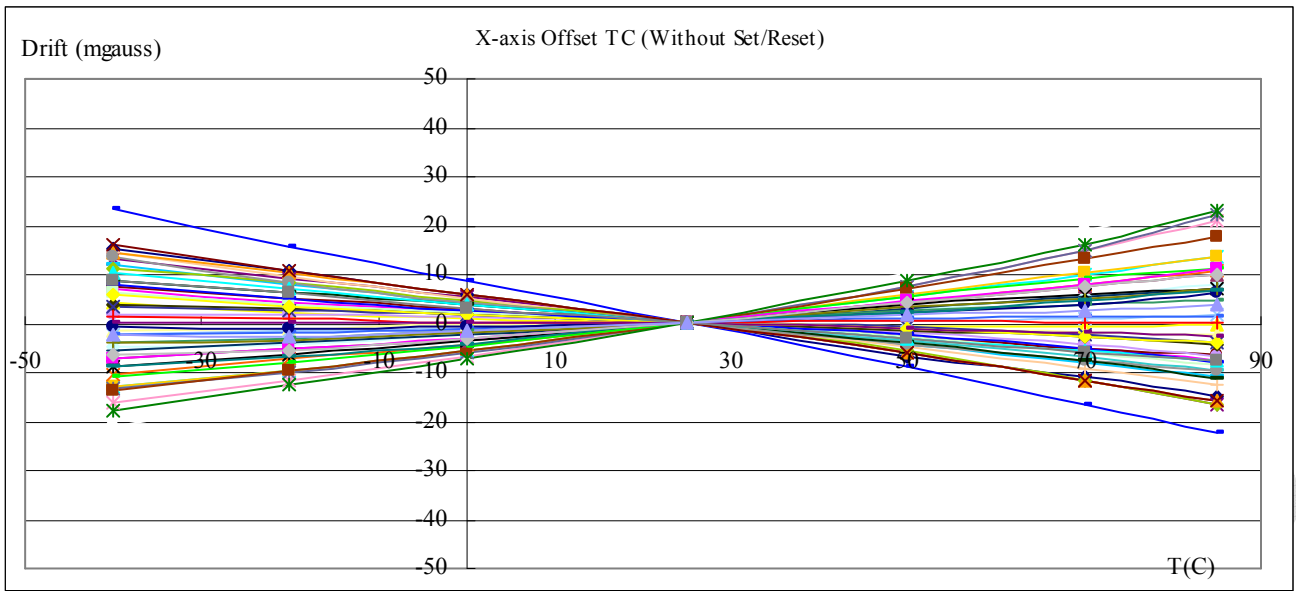
**Note:** Low Voltage Operation Mode means that the power supply (V<sub>DA</sub>) can be as low as 2.7V and that the part can function safely up to power supply voltages of 5.25V.

**TYPICAL CHARACTERISTICS, % OF UNITS (@ 25°C, V<sub>DD</sub> = 3V)**



# OVER TEMPERATURE CHARACTERISTICS





## PIN DESCRIPTIONS:

**V<sub>DA</sub>** – This is the supply input for the circuits and the magnetic sensor. The DC voltage should be between 2.7 and 5.25 volts. Refer to the section on PCB layout and fabrication suggestions for guidance on external parts and connections recommended.

**GND** – This is the ground pin for the magnetic sensor.

**SDA** – This pin is the I<sup>2</sup>C serial data line, and operates in FAST (400 KHz) mode.

**SCL** – This pin is the I<sup>2</sup>C serial clock line, and operates in FAST (400 KHz) mode.

**V<sub>DD</sub>** – This is the power supply input for the I<sup>2</sup>C bus, and is 1.8V compatible can be 1.62V to 5.25V.

**FM** – Factory use only, Leave Open/No Connect, internal pulled down.

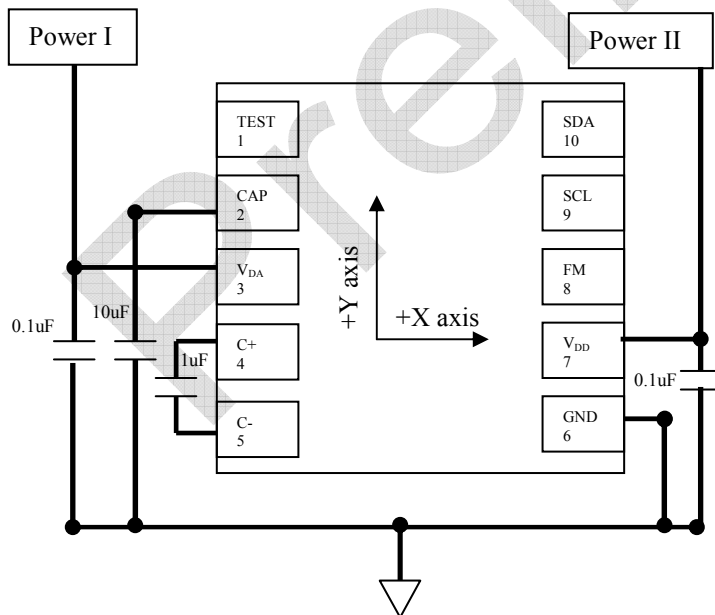
**TEST** – Factory use only, Leave Open/No Connect.

**CAP** – External capacitor pin for SET/RESET strap.

**C+, C-** – External capacitor pin, connect a 1uF capacitor across C+ and C-.

## EXTERNAL CAPACITOR CONNECTION

Two external low ESR ceramic capacitors are needed for proper SET/RESET operation of the magnetic sensor. A 10uF capacitor on the CAP pin and a 1uF capacitor across C+ and C- pin.



Low Voltage Operation Mode (Top View)

## POWER CONSUMPTION

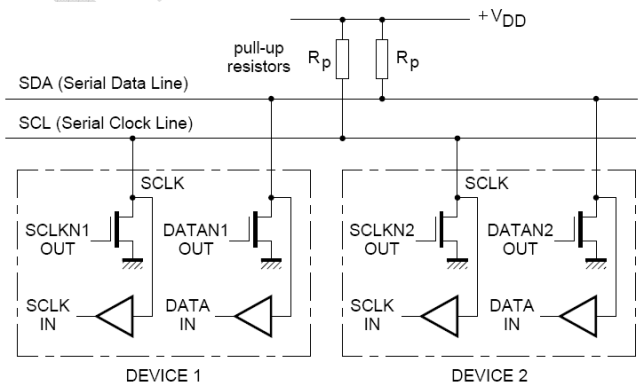
The MEMSIC magnetic sensor consumes 0.4mA (typical) current at 3V with 50 measurements/second, but the current is proportional to the measurements carried out, for example, if only 20 measurements/second are performed, the current will be  $0.4 \times 20 / 50 = 0.16\text{mA}$ .

## I<sup>2</sup>C INTERFACE DESCRIPTION

A slave mode I<sup>2</sup>C circuit has been implemented into the MEMSIC magnetic sensor as a standard interface for customer applications. The A/D converter and MCU functionality have been added to the MEMSIC sensor, thereby increasing ease-of-use, and lowering power consumption, footprint and total solution cost.

The I<sup>2</sup>C (or Inter IC bus) is an industry standard bi-directional two-wire interface bus. A master I<sup>2</sup>C device can operate READ/WRITE controls to an unlimited number of devices by device addressing. The MEMSIC magnetic sensor operates only in a slave mode, i.e. only responding to calls by a master device.

## I<sup>2</sup>C BUS CHARACTERISTICS



I<sup>2</sup>C Bus

The two wires in I<sup>2</sup>C bus are called SDA (serial data line) and SCL (serial clock line). In order for a data transfer to start, the bus has to be free, which is defined by both wires in a HIGH output state. Due to the open-drain/pull-up resistor structure and wired Boolean "AND" operation, any device on the bus can pull lines low and overwrite a HIGH signal. The data on the SDA line has to be stable during the HIGH period of the SCL line. In other words, valid data can only change when the SCL line is LOW.

Note: Rp selection guide: 4.7Kohm for a short I<sup>2</sup>C bus length (less than 4inches), and 10Kohm for less than 2inches I<sup>2</sup>C bus.



## DATA TRANSFER

A data transfer is started with a “START” condition and ended with a “STOP” condition. A “START” condition is defined by a HIGH to LOW transition on the SDA line while SCL line is HIGH. A “STOP” condition is defined by a LOW to HIGH transition on the SDA line while SCL line is HIGH. All data transfer in I<sup>2</sup>C system is 8-bits long. Each byte has to be followed by an acknowledge bit. Each data transfer involves a total of 9 clock cycles. Data is transferred starting with the most significant bit (MSB). After a “START” condition, master device calls specific slave device, in our case, a MEMSIC device with a 7-bit device address “[0110xx0]”. To avoid potential address conflict, either by ICs from other manufacturers or by other MEMSIC devices on the same bus, a total of **4 different addresses** can be pre-programmed into MEMSIC device by the factory. Following the 7-bit address, the 8<sup>th</sup> bit determines the direction of data transfer: [1] for READ and [0] for WRITE. After being addressed, available MEMSIC device being called should respond by an “Acknowledge” signal, which is pulling SDA line LOW.

In order to read sensor signal, master device should operate a WRITE action with a code of [xxxxxxx1] into MEMSIC device 8-bit internal register. Note that this action also serves as a “wake-up” call.

Bit	Name	Function
0	TM (Take Measurements)	Initiate measurement sequence for “1”, this bit will be cleared by circuit outside of I2C core after measurement and A/D are finished. More specifically, it will be automatically cleared by TM_DONE signal after the action is finished.
1	SET (Set Coil)	Writing “1” will set the MR by passing a large current through Set/Reset Coil. It will be automatically cleared by SETRESET_DONE signal after the action is finished.
2	RESET (Reset Coil)	Writing “1” will reset the MR by passing a large current through Set/Reset Coil in a reversed direction. It will be automatically cleared by SETRESET_DONE signal after the action is finished.
3	Reserved	
4	Reserved	
5	Reserved	
6	Reserved	

After writing code of [xxxxxxx1] into control register and a zero memory address pointer is also written, and if a “READ” command is received, the MEMSIC device being called transfers 8-bit data to I<sup>2</sup>C bus. If

“Acknowledge” by master device is received, MEMSIC device will continue to transfer next byte. The same procedure repeats until 5 byte of data are transferred to master device. Those 5 bytes of data are defined as following:

1. Internal register
2. MSB X-axis
3. LSB X-axis
4. MSB Y-axis
5. LSB Y-axis

Even though each axis consists two bytes, which are 16bits of data, the actual resolution is limited 12bits. Unused MSB should be simply filled by “0”s.

## POWER DOWN MODE

MEMSIC MR sensor will enter power down mode automatically after data acquisition is finished. A data acquisition is initiated when master writes in to the control register a code of [xxxxxxx1].

## EXAMPLE OF TAKE MEASUREMENT

First cycle: START followed by a calling to slave address [0110xx0] to WRITE (8<sup>th</sup> SCL, SDA keep low). [xx] is determined by factory programming, total 4 different addresses are available.

Second cycle: After a acknowledge signal is received by master device (MEMSIC device pulls SDA line low during 9<sup>th</sup> SCL pulse), master device sends “[00000000]” as the target address to be written into. MEMSIC device should acknowledge at the end (9<sup>th</sup> SCL pulse). Note: since MEMSIC device has only one internal register that can be written into, so user should always indicate “[00000000]” as the write address.

Third cycle: Master device writes to internal MEMSIC device memory the code “[00000001]” as a wake-up call to initiate a data acquisition. MEMSIC device should send acknowledge.

A STOP command indicates the end of write operation.

A minimal 5ms wait should be given to MEMSIC device to finish a data acquisition and return a valid output. The TM bit (Take Measurement bit in control register) will be automatically reset to “0” after data from A/D converter is ready. The transition from “1” to “0” of TM bit also indicates “data ready”. The device will go into sleep mode afterwards. Analog circuit will be powered off, but I<sup>2</sup>C portion will continue be active and data will not be lost.

Fourth cycle: Master device sends a START command followed by calling MEMSIC device address with a WRITE (8<sup>th</sup> SCL, SDA keep low). A ‘Acknowledge’ should be send by MEMSIC device at the end.

Fifth cycle: Master device writes to MEMSIC device a "[00000000]" as the starting address to read from internal memory. Since "[00000000]" is the address of internal control register, reading from this address can serve as a verification operation to confirm the write command has been successful. Note: the starting address in principle can be any of the 5 addresses. For example, user can start read from address [0000001], which is X channel MSB.

Sixth cycle: Master device calls MEMSIC device address with a READ (8<sup>th</sup> SCL cycle SDA line high). MEMSIC device should acknowledge at the end.

Seventh cycle: Master device cycles SCL line, first addressed memory data appears on SDA line. If in step 7, "[00000000]" was sent, internal control register data should appear (in the following steps, this case is assumed). Master device should send 'Acknowledge' at the end.

Eighth cycle: Master device continues cycle SCL line, next byte of internal memory should appear on SDA line (MSB of X channel). The internal memory address pointer automatically moves to the next byte. Master acknowledges.

Ninth cycle: LSB of X channel.

Tenth cycle: MSB of Y channel.

Eleventh cycle: LSB of Y channel.

Master ends communications by NOT sending 'Acknowledge' and also followed by a 'STOP' command.

#### **EXAMPLE OF SET/RESET COIL**

First cycle: START followed by a calling to slave address [0110xx0] to WRITE (8<sup>th</sup> SCL, SDA keep low). [xx] is determined by factory programming, total 4 different addresses are available.

Second cycle: After a acknowledge signal is received by master device (MEMSIC device pulls SDA line low

during 9<sup>th</sup> SCL pulse), master device sends "[00000000]" as the target address to be written into. MEMSIC device should acknowledge at the end (9<sup>th</sup> SCL pulse). Note: since MEMSIC device has only one internal register can be written into, user should always use "[00000000]" as the write address.

Third cycle: Master device writes to internal MEMSIC device memory a code "[00000010]" as a wake-up call to initiate a SET action, or a code "[00000100]" to initiate a RESET action. Note that in low voltage mode, master need to issue SET command if the previous command is RESET, and issue a RESET command if the previous command is SET. In the case of a cold start (device just powered on), master should only issue SET command. The wait time from power on to SET command should be a minimal 10ms. MEMSIC device should send acknowledge. Note that SET and RESET bits should not be set to "1" at the same time. In case of that happens, the device will only do a SET action. A STOP command indicates the end of write operation.

A minimal 50us wait period should be given to MEMSIC device to finish SET/RESET action before taking a measurement. The SET or RESET bit will be automatically reset to "0" after SET/RESET is done. And the device will go to sleep mode afterwards.

In low voltage operation mode, SET/RESET commands have to alternate. In other words, one can not do a SET following a SET, same for RESET. The first command after initial power up should be SET. If RESET command is attempted as the first command, it will be ignored. Between SET and RESET, a minimal 5ms need to be given for the voltage on capacitor to settle.

Note 1: at power-on, internal register and memory address pointer are reset to "0".

Note 2: In low voltage operation mode, device requires an additional capacitor to be able to do SET/RESET at lower supply voltage.

PACKAGE DRAWING

