

Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXV5004G series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This sensor combines a highly sensitive implanted strain gauge with advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

Features

- Temperature Compensated over 10° to 60°C
- Available in Gauge Surface Mount (SMT) or Through-Hole (DIP) Configurations
- Durable Thermoplastic (PPS) Package

Typical Applications

- Washing Machine Water Level
- Ideally Suited for Microprocessor or Microcontroller-Based Systems

ORDERING INFORMATION⁽¹⁾

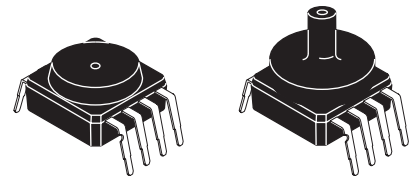
| Device Type | Case No. | MPXV Series Order No. | Packing Options | Device Marking |
|---------------|----------|-----------------------|-----------------|----------------|
| Through-Hole | 482B | MPXV5004G7U | Rails | MPXV5004G |
| | 482C | MPXV5004GC7U | Rails | MPXV5004G |
| Surface Mount | 482 | MPXV5004G6U | Rails | MPXV5004G |
| | 482 | MPXV5004G6T1 | Tape & Reel | MPXV5004G |
| | 482A | MPXV5004GC6U | Rails | MPXV5004G |
| | 482A | MPXV5004GC6T1 | Tape & Reel | MPXV5004G |
| | 1351 | MPXV5004DP | Trays | MPXV5004G |
| | 1368 | MPXV5004GVP | Trays | MPXV5004G |
| | 1369 | MPXV5004GP | Trays | MPXV5004G |

1. MPXV5004G series pressure sensors are available in the basic element package or with a pressure port. Two packing options are offered for the surface mount configuration.

MPXV5004G SERIES

**INTEGRATED
 PRESSURE SENSOR**
 0 TO 3.92 kPa
 (0 TO 400 mm H₂O)
 1.0 TO 4.9 V OUTPUT

SMALL OUTLINE PACKAGES THROUGH-HOLE



MPXV5004G7U
 CASE 482B-03

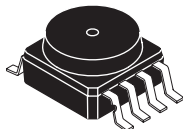
MPXV5004GC7U
 CASE 482C-03

PIN NUMBERS⁽¹⁾

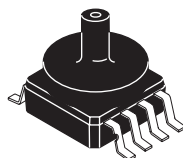
| | | | |
|---|------------------|---|-----|
| 1 | N/C | 5 | N/C |
| 2 | V _S | 6 | N/C |
| 3 | GND | 7 | N/C |
| 4 | V _{OUT} | 8 | N/C |

1. Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.

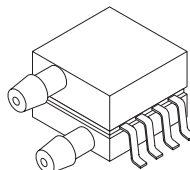
SMALL OUTLINE PACKAGES SURFACE MOUNT



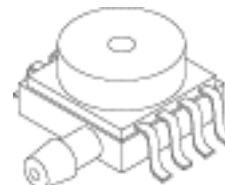
MPXV5004G6U
 CASE 482-01



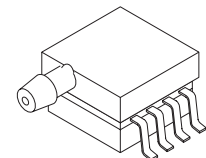
MPXV5004GC6U
 CASE 482A-01



MPXV5004DP
 CASE 1351-01



MPXV5004GVP
 CASE 1368-01



MPXV5004GP
 CASE 1369-01

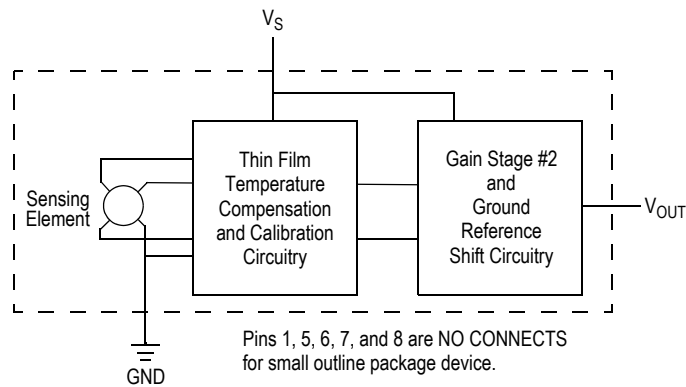


Figure 1. Fully Integrated Pressure Sensor Schematic

Table 1. Maximum Ratings⁽¹⁾

| Rating | Symbol | Value | Unit |
|----------------------------|------------------|-------------|------|
| Maximum Pressure (P1 > P2) | P _{MAX} | 16 | kPa |
| Storage Temperature | T _{STG} | -30 to +100 | °C |
| Operating Temperature | T _A | 0 to +65 | °C |

1. Exposure beyond the specified limits may cause permanent damage or degradation to the device.

Table 2. Operating Characteristics (V_S = 10 V_{DC}, T_A = 25°C unless otherwise noted, P1 > P2)

| Characteristic | Symbol | Min | Typ | Max | Units |
|--|------------------|------|------------|--------------|--|
| Pressure Range | P _{OP} | 0 | — | 3.92 400 | kPa mm H ₂ O |
| Supply Voltage ⁽¹⁾ | V _S | 4.75 | 5.0 | 5.25 | V _{DC} |
| Supply Current | I _S | — | — | 10 | mAdc |
| Span at 306 mm H ₂ O (3 kPa) ⁽²⁾ | V _{FSS} | — | 3.0 | — | V |
| Offset ^{(3) (4)} | V _{OFF} | 0.75 | 1.0 | 1.25 | mV |
| Sensitivity | V/P | — | 1.0 9.8 | — | V/kPa mV/mm H ₂ O |
| Accuracy ⁽⁵⁾ | — | — | — | ±1.5 ±2.5 | %V _{FSS} %V _{FSS} |

- Device is ratiometric within this specified excitation range.
- Span is defined as the algebraic difference between the output voltage at specified pressure and the output voltage at the minimum rated pressure.
- Offset (V_{off}) is defined as the output voltage at the minimum rated pressure.
- Accuracy (error budget) consists of the following:
 - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
 - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is cycled to and from the minimum or maximum operating temperature points, with zero differential pressure applied.
 - Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the minimum or maximum rated pressure, at 25°C.
 - Offset Stability: Output deviation, after 1000 temperature cycles, *30 to 100°C, and 1.5 million pressure cycles, with minimum rated pressure applied.
 - TcSpan: Output deviation over the temperature range of 10 to 60°C, relative to 25°C.
 - TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10 to 60°C, relative to 25°C.
 - Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V_{FSS}, at 25°C.
- Auto Zero at Factory Installation: Due to the sensitivity of the MPXV5004G, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ± 5°C between autozero and measurement.

ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPXV5004G series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and qualification test for dry air, and other media, are available

from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the MPXV5004G to the A/D input of the microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

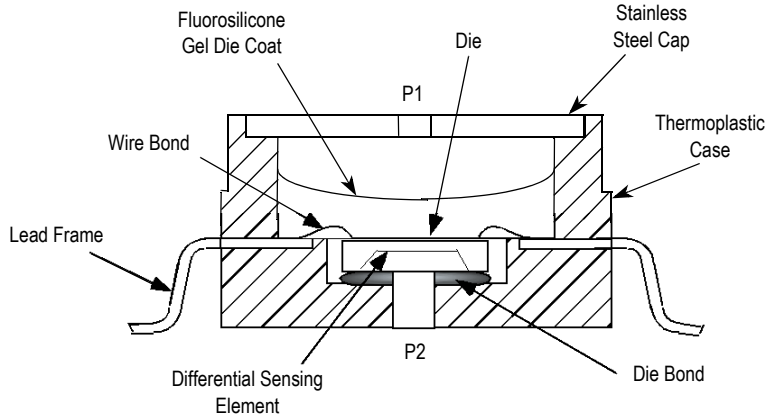


Figure 2. Cross-Sectional Diagram (Not to Scale)

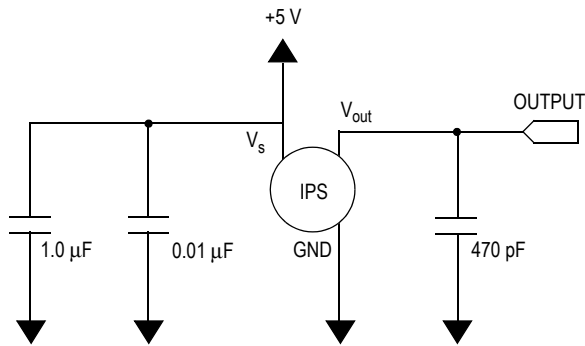


Figure 3. Recommended Power Supply Decoupling and Output Filtering.

(For additional output filtering, please refer to Application Note AN1646.)

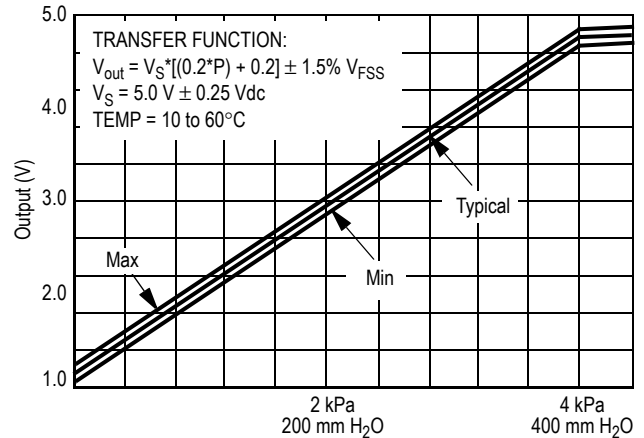


Figure 4. Output versus Pressure Differential (See Note 5 in Operating Characteristics)

PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale Semiconductor designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing the silicone gel which isolates the die from the environment. The

Freescale Semiconductor pressure sensor is designed to operate with positive differential pressure applied, $P1 > P2$.

The Pressure (P1) side may be identified by using the table below.

| Part Number | Case Type | Pressure (P1) Side Identifier |
|-----------------|-----------|-------------------------------|
| MPXV5004GC6U/T1 | 482A | Side with Port Attached |
| MPXV5004G6U/T1 | 482 | Stainless Steel Cap |
| MPXV5004GC7U | 482C | Side with Port Attached |
| MPXV5004G7U | 482B | Stainless Steel Cap |
| MPXV5004GP | 1369 | Side with Port Attached |
| MPXV5004DP | 1351 | Side with Port Marking |
| MPXV5004GVP | 1368 | Stainless Steel Cap |

INFORMATION FOR USING THE SMALL OUTLINE PACKAGE (CASE 482)

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface

between the board and the package. With the correct footprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

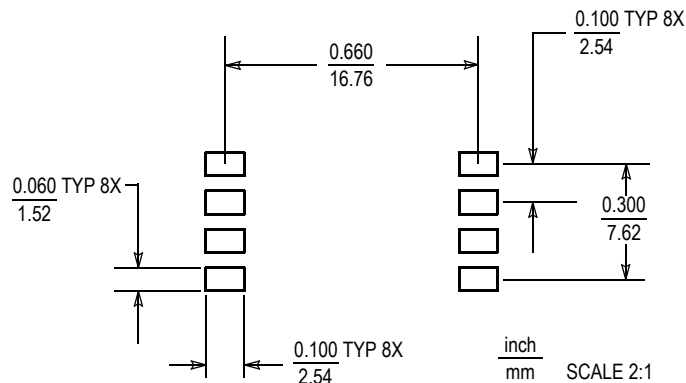
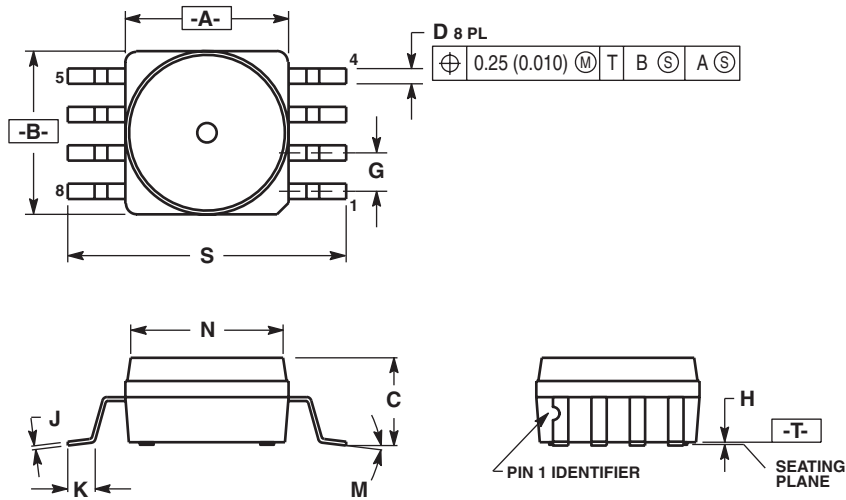


Figure 5. SOP Footprint (Case 482)

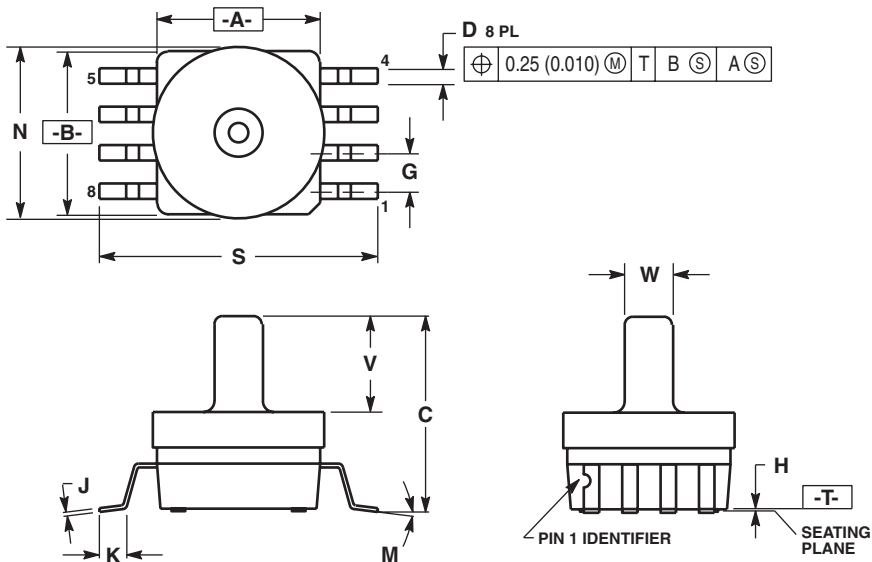
PACKAGE DIMENSIONS



**CASE 482-01
ISSUE O
SMALL OUTLINE PACKAGE
SURFACE MOUNT**

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.212 | 0.230 | 5.38 | 5.84 |
| D | 0.038 | 0.042 | 0.96 | 1.07 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.002 | 0.010 | 0.05 | 0.25 |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.061 | 0.071 | 1.55 | 1.80 |
| M | 0" | 7" | 0" | 7" |
| N | 0.405 | 0.415 | 10.29 | 10.54 |
| S | 0.709 | 0.725 | 18.01 | 18.41 |

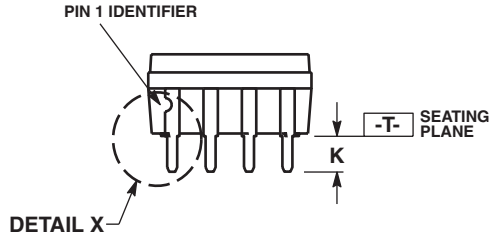
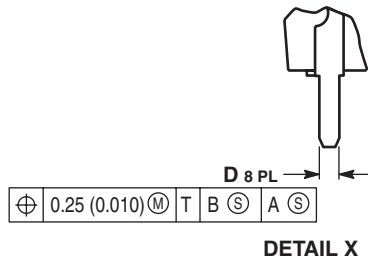
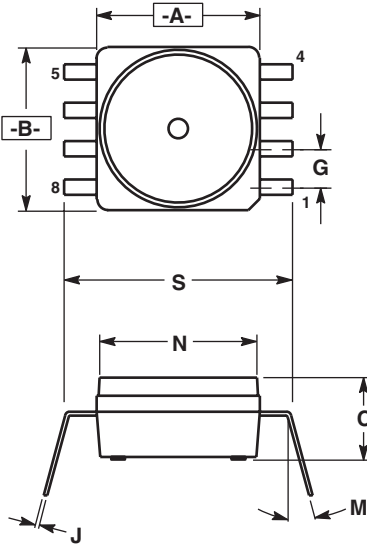


**CASE 482A-01
ISSUE A
SMALL OUTLINE PACKAGE
SURFACE MOUNT**

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
 5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.500 | 0.520 | 12.70 | 13.21 |
| D | 0.038 | 0.042 | 0.96 | 1.07 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.002 | 0.010 | 0.05 | 0.25 |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.061 | 0.071 | 1.55 | 1.80 |
| M | 0" | 7" | 0" | 7" |
| N | 0.444 | 0.448 | 11.28 | 11.38 |
| S | 0.709 | 0.725 | 18.01 | 18.41 |
| V | 0.245 | 0.255 | 6.22 | 6.48 |
| W | 0.115 | 0.125 | 2.92 | 3.17 |

PACKAGE DIMENSIONS

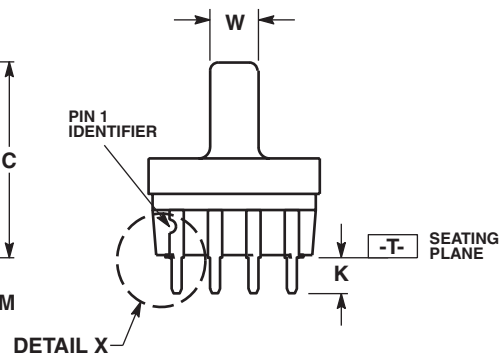
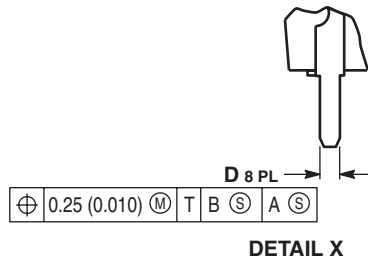
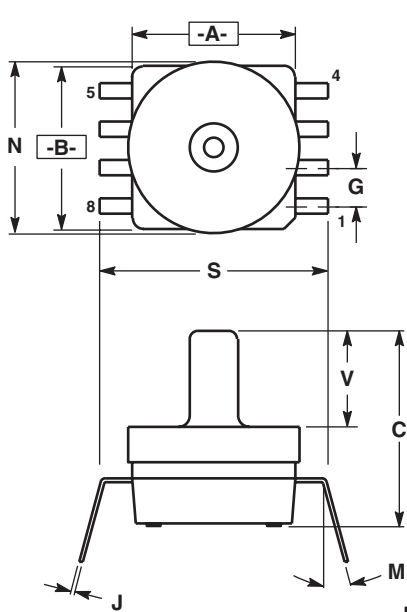


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.210 | 0.220 | 5.33 | 5.59 |
| D | 0.026 | 0.034 | 0.66 | 0.864 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.100 | 0.120 | 2.54 | 3.05 |
| M | 0° | 15° | 0° | 15° |
| N | 0.405 | 0.415 | 10.29 | 10.54 |
| S | 0.540 | 0.560 | 13.72 | 14.22 |

CASE 482B-03 ISSUE B SMALL OUTLINE PACKAGE THROUGH-HOLE



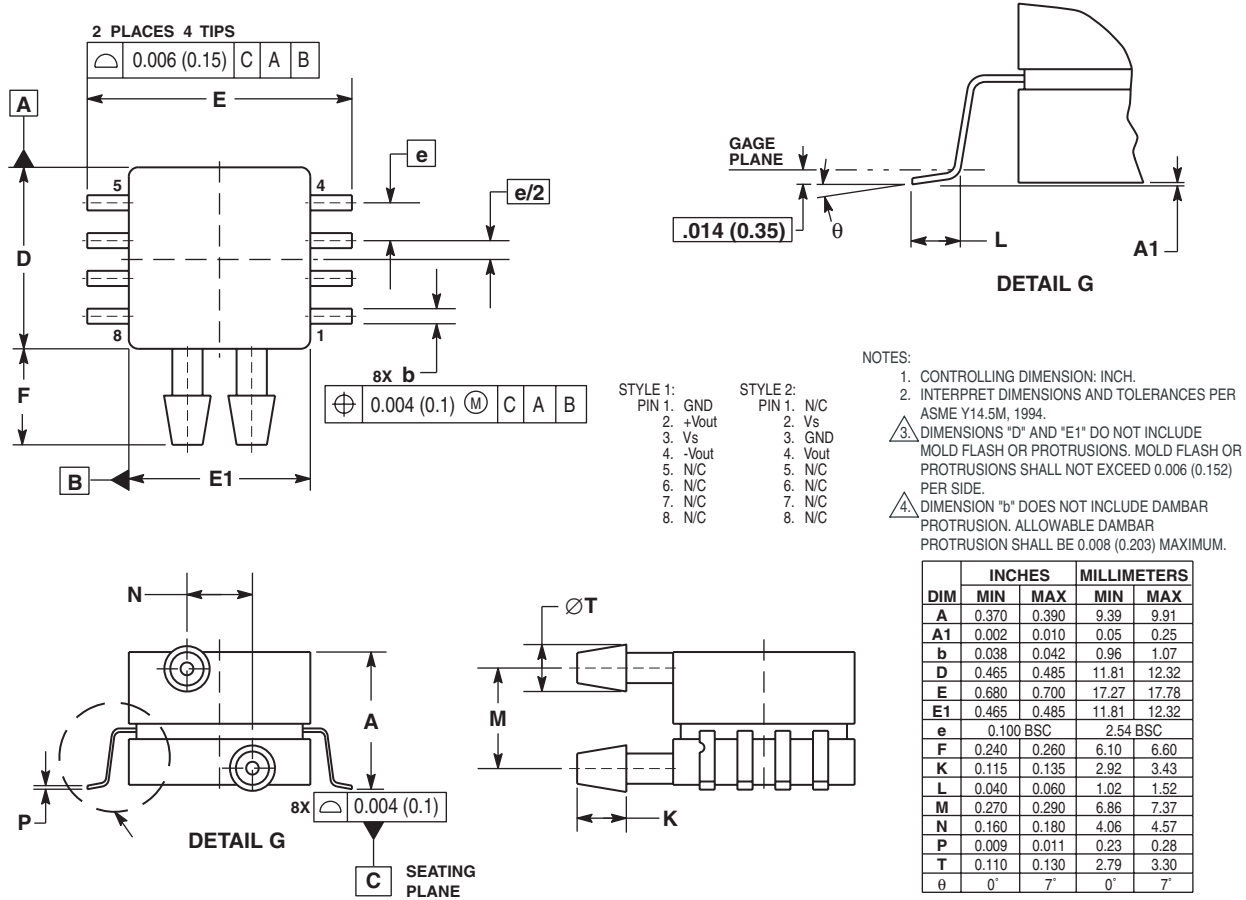
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006).
5. ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
6. DIMENSION S TO CENTER OF LEAD WHEN FORMED PARALLEL.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.415 | 0.425 | 10.54 | 10.79 |
| B | 0.415 | 0.425 | 10.54 | 10.79 |
| C | 0.500 | 0.520 | 12.70 | 13.21 |
| D | 0.026 | 0.034 | 0.66 | 0.864 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.009 | 0.011 | 0.23 | 0.28 |
| K | 0.100 | 0.120 | 2.54 | 3.05 |
| M | 0° | 15° | 0° | 15° |
| N | 0.444 | 0.448 | 11.28 | 11.38 |
| S | 0.540 | 0.560 | 13.72 | 14.22 |
| V | 0.245 | 0.255 | 6.22 | 6.48 |
| W | 0.115 | 0.125 | 2.92 | 3.17 |

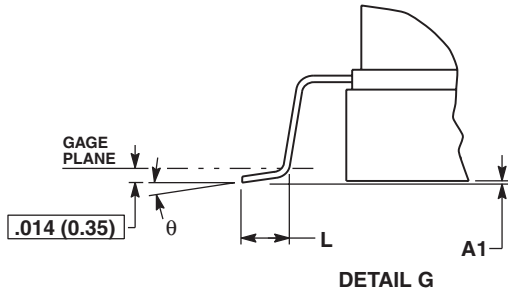
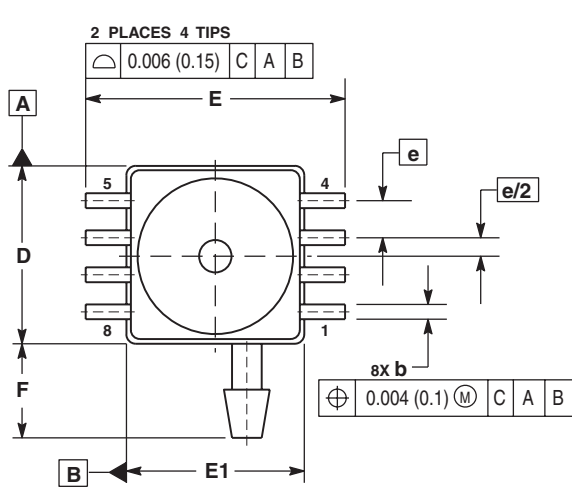
CASE 482C-03 ISSUE B SMALL OUTLINE PACKAGE THROUGH-HOLE

PACKAGE DIMENSIONS

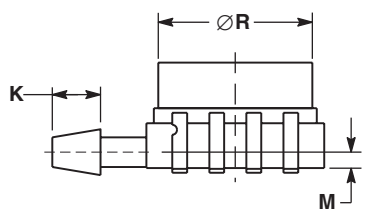
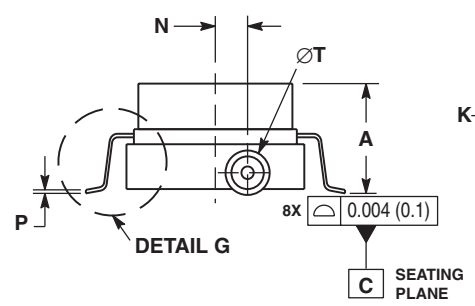


CASE 1351-01 ISSUE O SMALL OUTLINE PACKAGE SURFACE MOUNT

PACKAGE DIMENSIONS



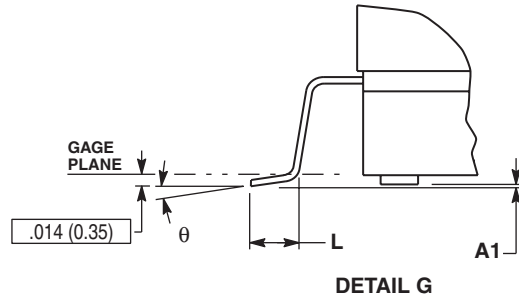
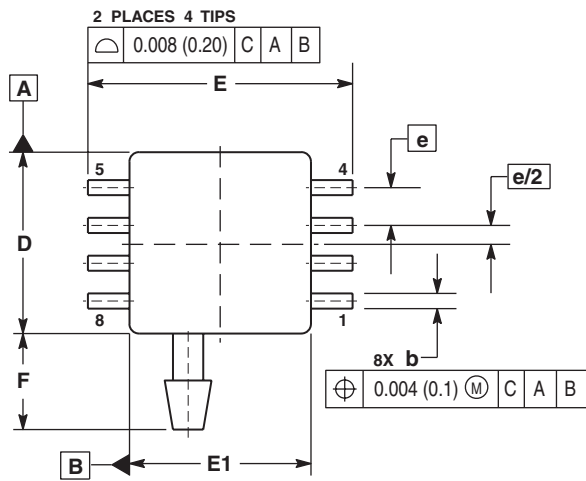
- NOTES:
 1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE.
 4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.008 (0.203) MAXIMUM.
- | | |
|------------|------------|
| STYLE 1: | STYLE 2: |
| PIN 1: GND | PIN 1: N/C |
| 2: +Vout | 2: Vs |
| 3: Vs | 3: GND |
| 4: -Vout | 4: Vout |
| 5: N/C | 5: N/C |
| 6: N/C | 6: N/C |
| 7: N/C | 7: N/C |
| 8: N/C | 8: N/C |



| DIM | INCHES | | MILLIMETERS | |
|----------|--------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.280 | 0.300 | 7.11 | 7.62 |
| A1 | 0.002 | 0.010 | 0.05 | 0.25 |
| b | 0.038 | 0.042 | 0.96 | 1.07 |
| D | 0.465 | 0.485 | 11.81 | 12.32 |
| E | 0.690 | BSC | 17.52 | BSC |
| E1 | 0.465 | 0.485 | 11.81 | 12.32 |
| e | 0.100 | BSC | 2.54 | BSC |
| F | 0.240 | 0.260 | 6.10 | 6.60 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.040 | 0.060 | 1.02 | 1.52 |
| M | 0.035 | 0.055 | 0.89 | 1.39 |
| N | 0.075 | 0.095 | 1.90 | 2.41 |
| P | 0.009 | 0.011 | 0.23 | 0.28 |
| T | 0.110 | 0.130 | 2.79 | 3.30 |
| R | 0.405 | 0.415 | 10.28 | 10.54 |
| θ | 0° | 7° | 0° | 7° |

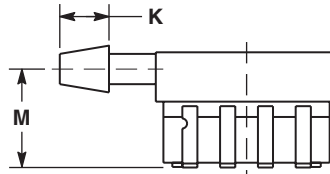
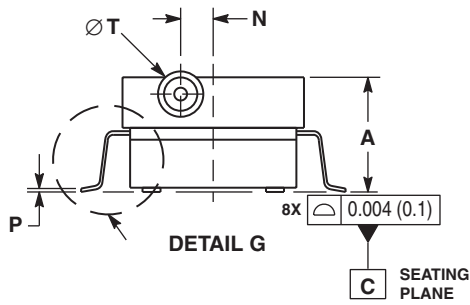
CASE 1368-01 ISSUE O SMALL OUTLINE PACKAGE SURFACE MOUNT

PACKAGE DIMENSIONS



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 (0.152) PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.008 (0.203) MAXIMUM.



| DIM | INCHES | | MILLIMETERS | |
|----------|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.300 | 0.330 | 7.11 | 7.62 |
| A1 | 0.002 | 0.010 | 0.05 | 0.25 |
| b | 0.038 | 0.042 | 0.96 | 1.07 |
| D | 0.465 | 0.485 | 11.81 | 12.32 |
| E | 0.717 BSC | | 18.21 BSC | |
| E1 | 0.465 | 0.485 | 11.81 | 12.32 |
| e | 0.100 BSC | | 2.54 BSC | |
| F | 0.245 | 0.255 | 6.22 | 6.47 |
| K | 0.120 | 0.130 | 3.05 | 3.30 |
| L | 0.061 | 0.071 | 1.55 | 1.80 |
| M | 0.270 | 0.290 | 6.86 | 7.36 |
| N | 0.080 | 0.090 | 2.03 | 2.28 |
| P | 0.009 | 0.011 | 0.23 | 0.28 |
| T | 0.115 | 0.125 | 2.92 | 3.17 |
| θ | 0° | 7° | 0° | 7° |

CASE 1369-01 ISSUE O SMALL OUTLINE PACKAGE SURFACE MOUNT



NOTES

NOTES

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