MN74HC162/MN74HC162S

Synchronous Decade Counter with Synchronous Clear

■ Outline

The MN74HC162/MN74HC162S is a presettable synchronous decimal counter. It has adopted the internal carry look ahead system so that is also serve as a high speed counter. The output of every flip-flop changes at the rising edge of the clock input.

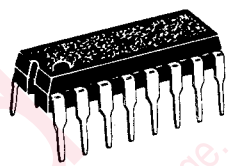
The counter output can be optionally preset into either the "H" level or the "L" level by using the load inpt because this counter is entirely programmable. The four flip-flops are preset synchronously with the rising edge of the clock input. When level of the load input is "L", the counter stops its function, and data corresponding to the input data to be set with the next clock pulse appears on the output irrespectively of the enable input level. The counter does not function even if the level of the load input becomes "H" before detection of the rising edge of the clock input. The clear function is synchronized with the clock input, and when the level of the clear input is "L", the clear function works at the rising edge of the clock input.

The carry look ahead circuit is used for cascade connection of the n-bit synchronous counter without any additional parts. It is the two active "High" enable inputs (ENP, ENT) and the ripple carry (RC) output that fulfill this function. When the levels of the enable inputs ENP and ENT are both "H", the counting function remains valid. The width of the ripple carry output is almost the same as of the "H" level of the output Q_A. The overflow ripple carry pulse of the "H" level can sequentially enable each stage connected with the cascade.

Owing to the silicon gate CMOS process, this decimal counter has realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL, and can directly drive ten LS TTL inputs.

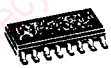
To protect the input and output against electrostatic breakdown, a resistor and a diode areused for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

P-3



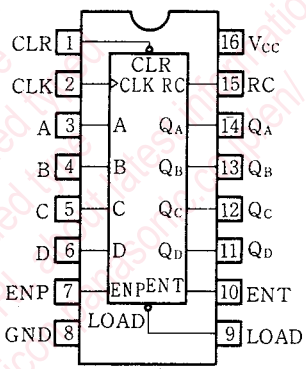
16-pin plastic DIL package

P-4



16-pin PANAFLAT package (SO-16D)

Pin Configuration

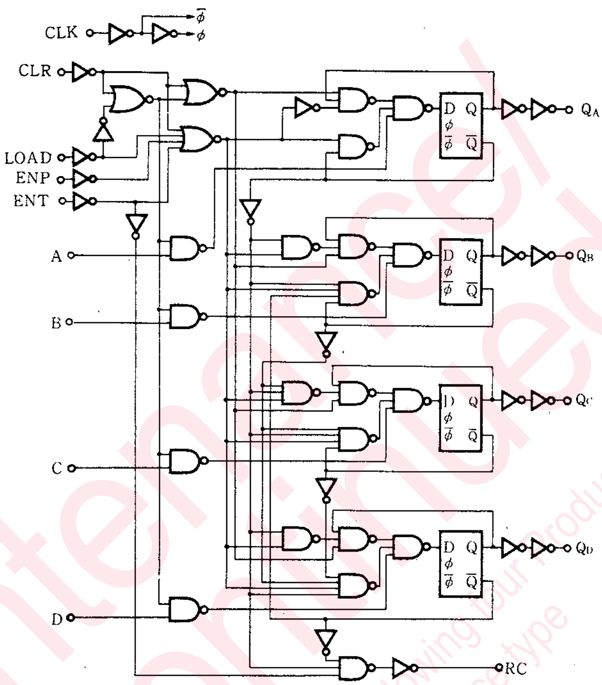


■ Truth Table

CLK	CLR	ENP	ENT	LOAD	Output
↓	L	×	×	×	Clear
×	H	H	L	H	Count & RC disabled
×	H	L	H	H	Count disabled
×	H	L	L	H	Count & RC disabled
↓	H	×	×	L	Load
↓	H	H	H	H	Increment Counter

Note) 1. ↓ : In leading of clock from "L" to "H" increment count is performed. When loard is "L" input data are loaded.
2. × : "H" or "L" either will do.

■ Logic Diagram



■ Absolute Maximum Ratings

Item			Symbol	Rating	Unit
Supply voltage			V_{CC}	−0.5～+7.0	V
Input output voltage			V_I, V_O	−0.5～V_{CC}+0.5	V
Input protective diode current			I_{IK}	±20	mA
Output parasitic diode current			I_{OK}	±20	mA
Output current			I_O	±25	mA
Supply current			I_{CC}, I_{GND}	±50	mA
Storage temperature			T_{stg}	−65～+150	°C
Power dissipation	MN74HC162	Ta=−40～+60°C	P_D	400	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC162S	Ta=−40～+60°C	P_D	275	mW
		Ta=+60～+85°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item	Symbol	V_{CC}(V)	Rating	Unit
Operating power supply voltage	V_{CC}		1.4～6.0	V
Input output voltage	V_I, V_O		0～V_{CC}	V
Operating temperature	T_A		−40～+85	°C
Input rise, fall time	t_r, t_f	2.0	0～1000	ns
		4.5	0～500	ns
		6.0	0～400	ns

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■ DC Characteristics (GND=0V)

Item	Symbol	V_{CC} (V)	Test Condition V_I	Test Condition V_O	Test Condition Unit	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0	V_{IH} or V_{IL}	−20.0	μA	1.9	2.0		1.9		V
		4.5		−20.0	μA	4.4	4.5		4.4		
		6.0		−20.0	μA	5.9	6.0		5.9		
		4.5		−4.0	mA	3.92			3.84		
		6.0		−5.2	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0	V_{IH} or V_{IL}	20.0	μA		0.0	0.1		0.1	V
		4.5		20.0	μA		0.0	0.1		0.1	
		6.0		20.0	μA		0.0	0.1		0.1	
		4.5		4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I_I	6.0	$V_I=V_{CC}$ or GND					±0.1		±1.0	μA
Static supply current	I_{CC}	6.0	$V_I=V_{CC}$ or GND, $I_O=0$					8.0		80.0	μA

■ AC Characteristics (GND=0V, Input transition time≦6ns, C_L=50pF)

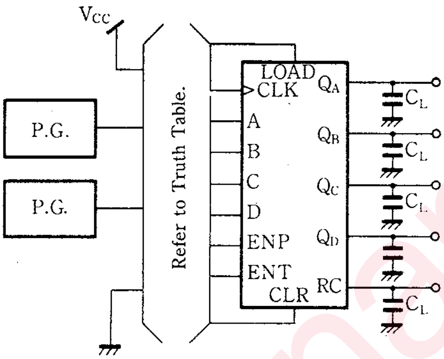
Item	Symbol	V_{CC} (V)	Test Condition	Ta=25°C min.	Ta=25°C typ.	Ta=25°C max.	Ta=−40~+85°C min.	Ta=−40~+85°C max.	Unit
Output rise time	t_{TLH}	2.0			25	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			20	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD="H"		43	175		220	ns
		4.5			7	35		44	
		6.0			15	30		37	
Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD="H"		39	175		220	ns
		4.5			16	35		44	
		6.0			14	30		37	
Propagation time CLK→Q_A~Q_D (L→H)	t_{PLH}	2.0	LOAD="L"		42	175		220	ns
		4.5			17	35		44	
		6.0			14	30		37	
Propagation time CLK→Q_A~Q_D (H→L)	t_{PHL}	2.0	LOAD="L"		38	175		220	ns
		4.5			16	35		44	
		6.0			14	30		37	

■ AC Characteristics (cont.)

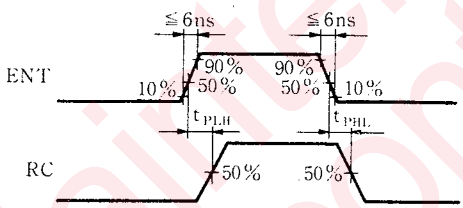
Item	Symbol	V_{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Propagation time CLK→RC (L→H)	t_{PLH}	2.0			53	200		250	ns
		4.5			23	40		50	
		6.0			19	34		43	
Propagation time CLK→RC (H→L)	t_{PHL}	2.0			46	200		250	ns
		4.5			20	40		50	
		6.0			16	34		43	
Propagation time ENT→RC (L→H)	t_{PLH}	2.0			33	150		190	ns
		4.5			13	30		38	
		6.0			11	26		33	
Propagation time ENT→RC (H→L)	t_{PHL}	2.0			38	175		220	ns
		4.5			15	35		44	
		6.0			12	30		37	
Minimum set-up time LOAD	t_{su}	2.0			34	125		155	ns
		4.5			11	25		31	
		6.0			8	21		26	
Minimum set-up time A, B, C, D	t_{su}	2.0			36	100		125	ns
		4.5			6	20		25	
		6.0			4	17		21	
Minimum set-up time CLR	t_{su}	2.0			36	125		155	ns
		4.5			10	25		31	
		6.0			8	21		26	
Minimum hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum pulse width CLK	t_w	2.0			36	100		125	ns
		4.5			11	20		25	
		6.0			8	17		21	
Maximum clock frequency	f_{max}	2.0		6	15		5		MHz
		4.5		30	56		24		
		6.0		35	66		28		

- Switching time measuring circuit and waveforms

1. Measuring circuit

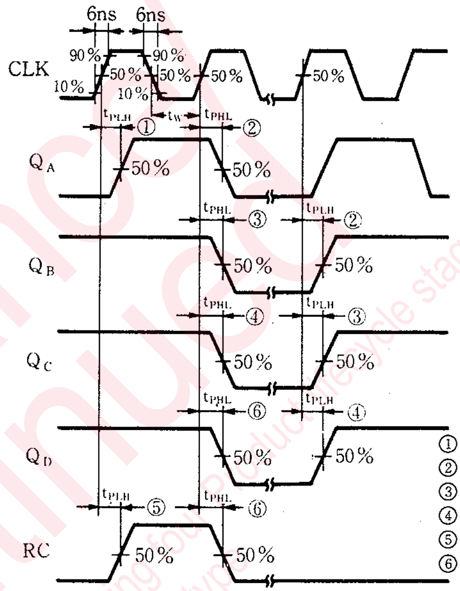


2 t_{PLH}, t_{PHL} (ENT→RC)



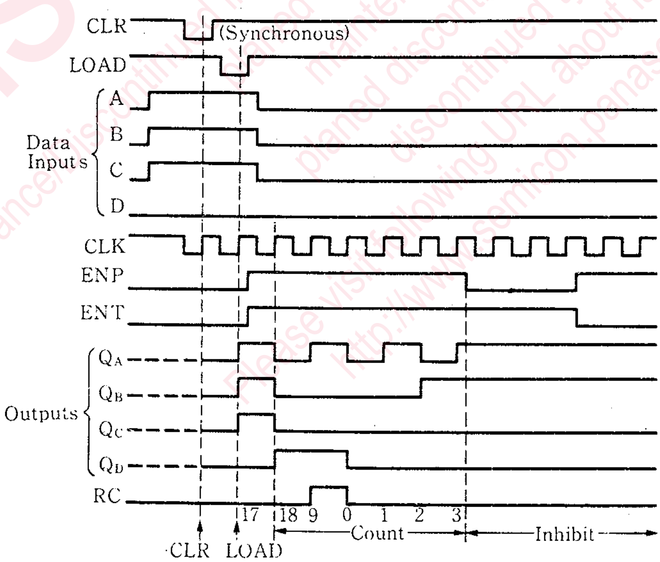
2. Switching waveforms

1 t_{PLH}, t_{PHL} (CLK→Q_A~Q_D, RC)



① Measured at t_{n+1}
② Measured at t_{n+2}
③ Measured at t_{n+4}
④ Measured at t_{n+8}
⑤ Measured at t_{n+15}
⑥ Measured at t_{n+16}

■ Typical Operating Condition



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