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# HD74HC137

3-to-8-line Decoder/Demultiplexer with Address Latch

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## Description

The HD74HC137 implements a three-to-eight line decoder with latches on the three address inputs. When  $\overline{GL}$  goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as  $\overline{GL}$  remains high no address changes will be recognized. Output enable controls,  $G_1$  and  $\overline{G_2}$ , control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless  $G_1$  is high and  $\overline{G_2}$  is low. The HD74HC137 is ideally suited for the implementation of glitchfree decoders in stored-address applications in bus oriented systems.

## Features

- High Speed Operation:  $t_{pd}$  (A, B, C to Y) = 16.5 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  V to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )

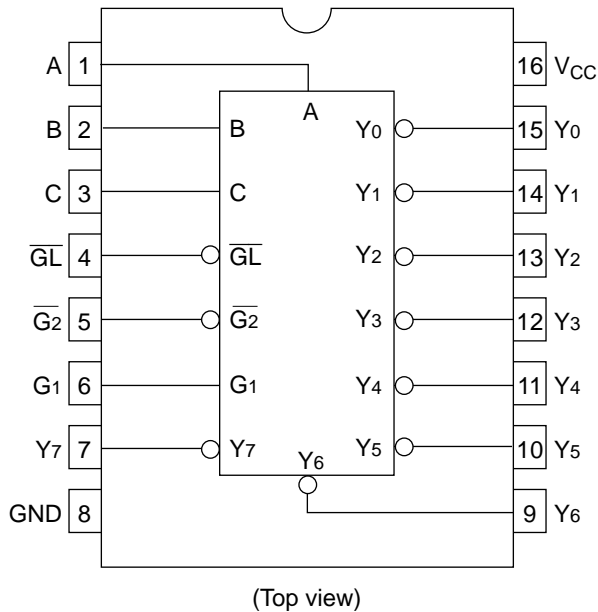
# HD74HC137

## Function Table

### Inputs

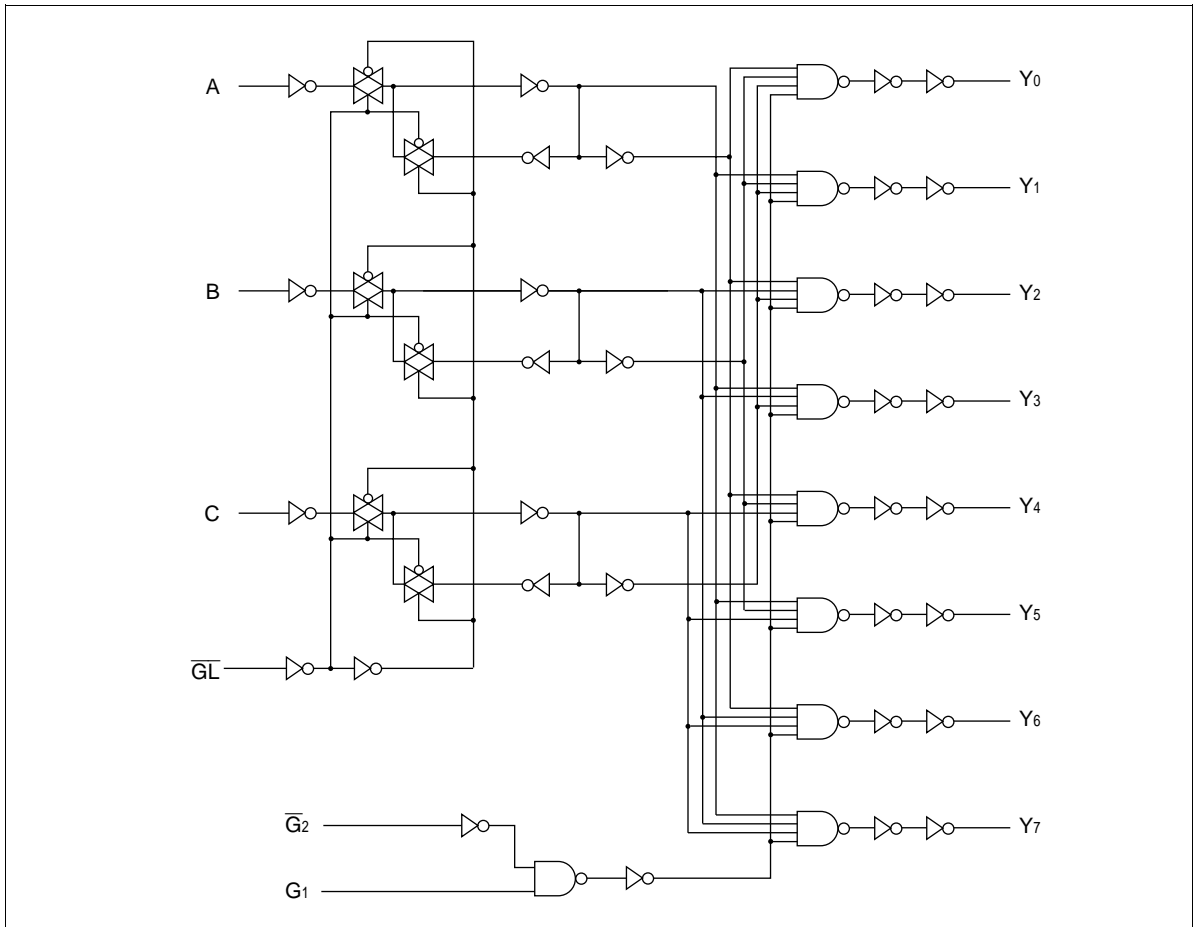
Enable			Select			Outputs							
$\overline{G_L}$	$G_1$	$\overline{G_2}$	C	B	A	$Y_0$	$Y_1$	$Y_2$	$Y_3$	$Y_4$	$Y_5$	$Y_6$	$Y_7$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to stored address L; all Others. H							

## Pin Arrangement



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Block Diagram



## DC Characteristics

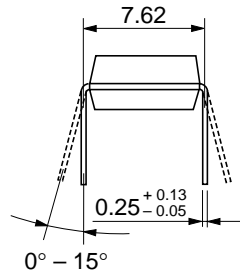
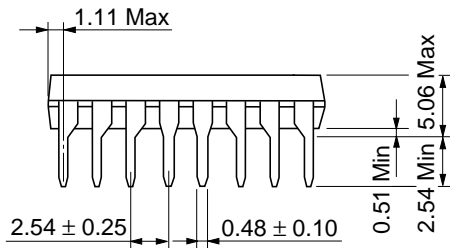
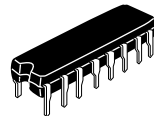
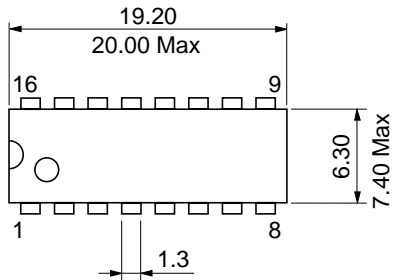
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5		V
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I <sub>OH</sub> = -4 mA
		6.0	5.68	—	—	5.63	—		I <sub>OH</sub> = -5.2 mA
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	Vin = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33		I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA

AC Characteristics ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

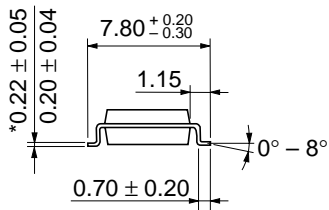
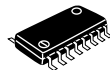
Item	Symbol	$V_{CC}$ (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions			
			Min	Typ	Max	Min			Max		
Propagation delay time	$t_{PLH}$	2.0	—	—	170	—	215	ns	A, B or C to Y		
		4.5	—	16	34	—	43				
		6.0	—	—	29	—	37				
	$t_{PHL}$	2.0	—	—	240	—	300				
		4.5	—	17	48	—	60				
		6.0	—	—	41	—	51				
	$t_{PLH}$	2.0	—	—	130	—	165			ns	$\overline{G}_2$ to Y
		4.5	—	13	26	—	33				
		6.0	—	—	22	—	28				
	$t_{PHL}$	2.0	—	—	195	—	245			ns	
		4.5	—	14	39	—	49				
		6.0	—	—	33	—	42				
	$t_{PLH}$	2.0	—	—	150	—	190			ns	$G_1$ to Y
		4.5	—	14	30	—	38				
		6.0	—	—	26	—	33				
	$t_{PHL}$	2.0	—	—	195	—	245			ns	
		4.5	—	14	39	—	49				
		6.0	—	—	33	—	42				
$t_{PLH}$	2.0	—	—	175	—	220	ns	$\overline{G_L}$ to Y			
	4.5	—	17	35	—	44					
	6.0	—	—	30	—	37					
$t_{PHL}$	2.0	—	—	250	—	315	ns				
	4.5	—	18	50	—	63					
	6.0	—	—	43	—	54					
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	A, B, C inputs		
		4.5	20	3	—	25	—				
		6.0	17	—	—	21	—				
Hold time	$t_h$	2.0	50	—	—	65	—	ns	A, B, C inputs		
		4.5	10	-3	—	13	—				
		6.0	9	—	—	11	—				

**AC Characteristics** ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns) (Cont)

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	$t_{TLH}$ $t_{THL}$	2.0	—	—	75	—	90	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g





\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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